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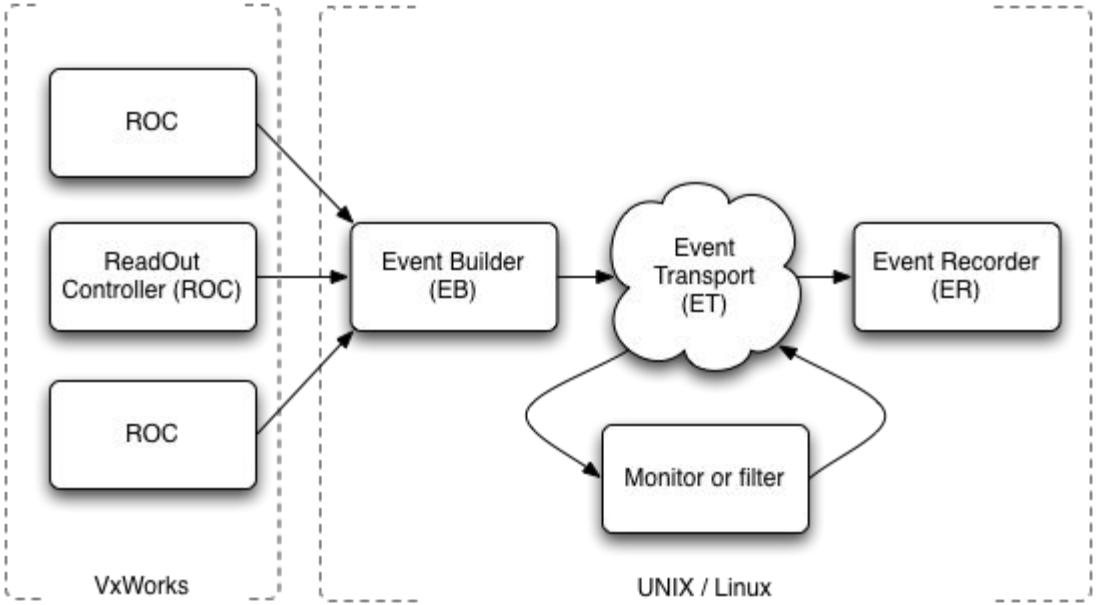
CODA basics

Currently to take data we use RCDAQ as a Data acquisition system. JLab will primarily use CODA so it is good to familiarize ourselves with it. We are waiting on a computer to do such work on as well as a trigger interface PCIe card which will work with existing SRS at SBU and CODA software.

CODA (**C**EBAF **O**nline **D**ata **A**cquisition) can have a few detector channels or tens of thousands

Example CODA layout implementation



1. Data is taken by detectors
2. Front end converter digitizes data (hardware complements assist)
3. Data can be observed and analyzed

Hardware+other specifications

PCIecard is an example of a trigger interface used by CODA which we will be using. It is important because custom hardware is expensive and unnecessary.

CentOS7 for VMEs (both are the typical software and environment, respectively, for CODA). Run Control controls and monitors experiments and the graphical editor is jCedit.

EVIO is the native CODA data format and allows manipulation from C, C++, and Java

Event Transfer can send data buffers between programs.

HADES basics

The CTS (Central Trigger System) is a VHDL module in the central FPGA of *one* TRB3 in the system (could also be on a different hardware, but we can combine all on one TRB3). This module takes the external (and internal) trigger sources and generates out of them a timing signal and the needed internal TRBNet trigger, which is then transported to all slaves (which in our case are all on the same TRB3). They react on the trigger and extract the data from the front end and transport it to the central FPGA, which is your *special* case (only one TRB3) is the same FPGA as the CTS is running in. There the data is collected from all 4 peripheral FPGAs and then combined to a UDP-frame, which is then sent via many Ethernet-packets to the Eventbuilder.

HADES basics

GSI in Germany centers their DAQ mainly around an FPGA system called TRBs.

1. Data readout from several TRBs and events building.
2. If necessary, sort incoming UDP packets according trigger number. Enables usage of TRB3 with two Ethernet links.
3. Store data in HLD files
4. Deliver data for arbitrary online analysis via GSI-standard socket connection (so-called MBS stream server)

Then analysis can occur

DiRICH5s1 (DiRICH5 standalone)

The DiRICH5s1 is just like the DiRICH3-5, but it its own optical transceiver and the power connector (with trigger and clock) on board, therefore it is standalone and doesn't need a backplane.