HRPPDs
for EIC Cherenkov detectors

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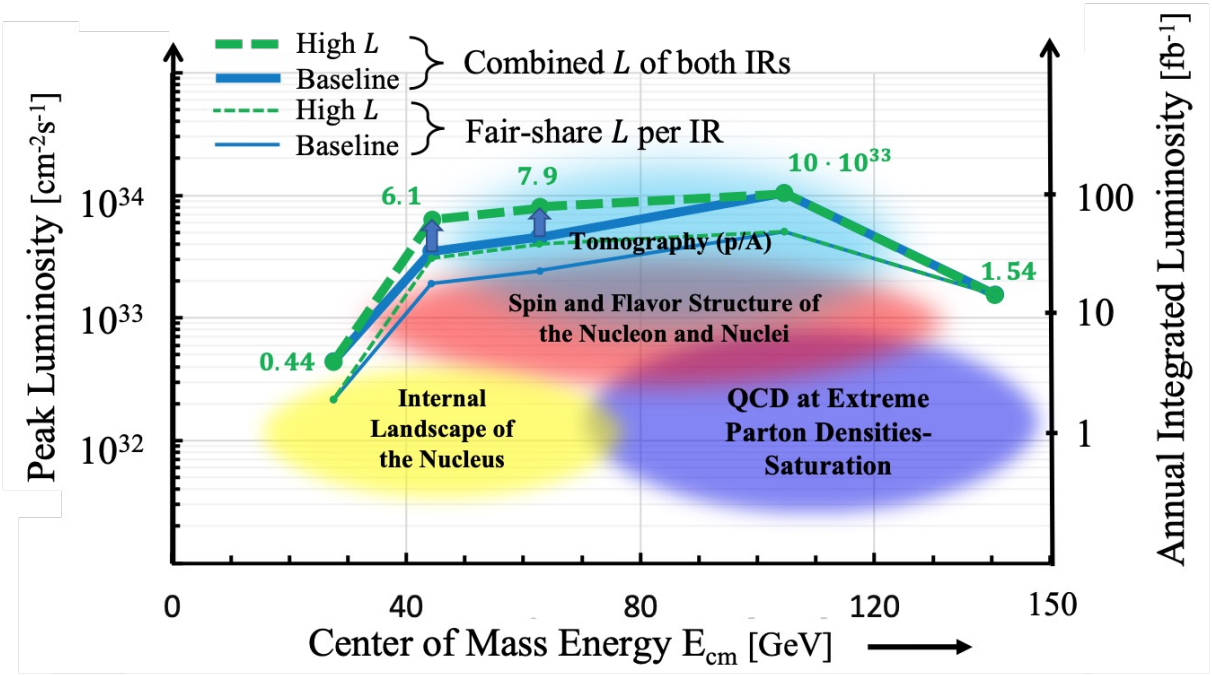
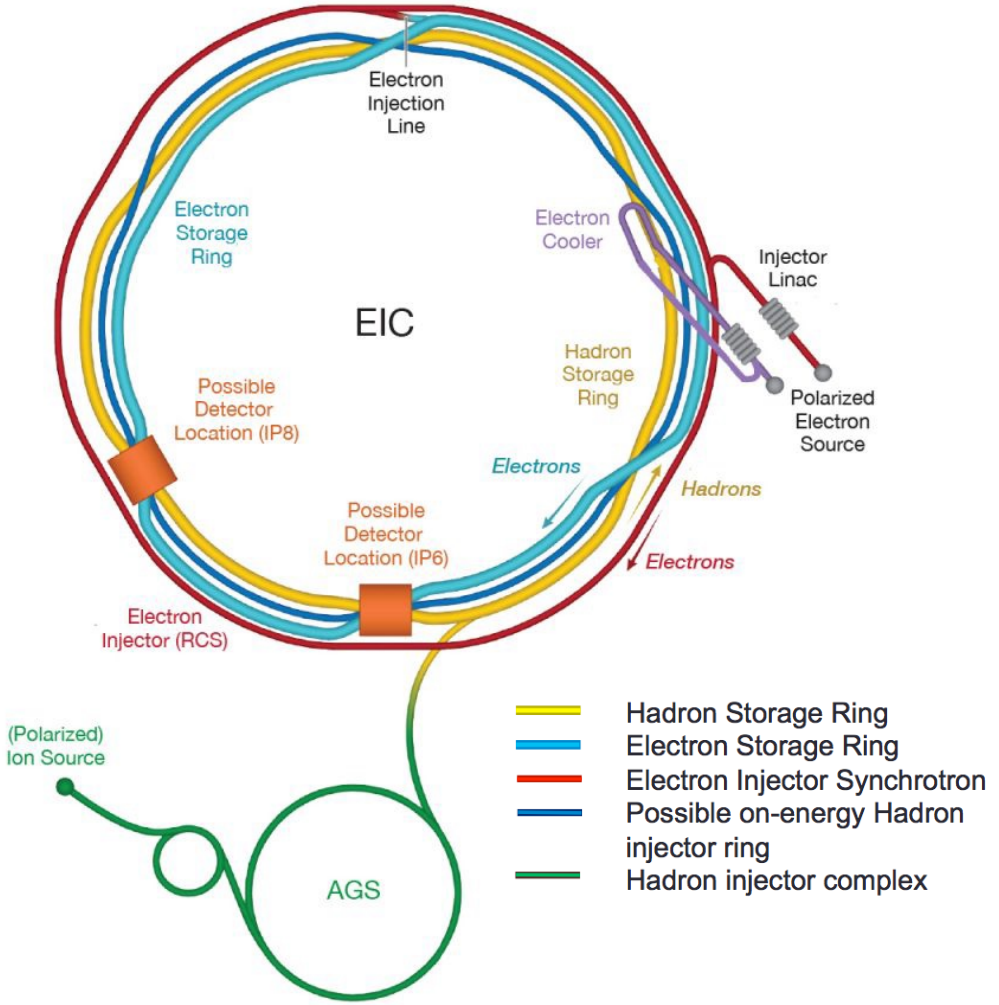
LAPPD / HRPPD Workshop #4, May 8, 2024

Electron-Ion Collider at Brookhaven

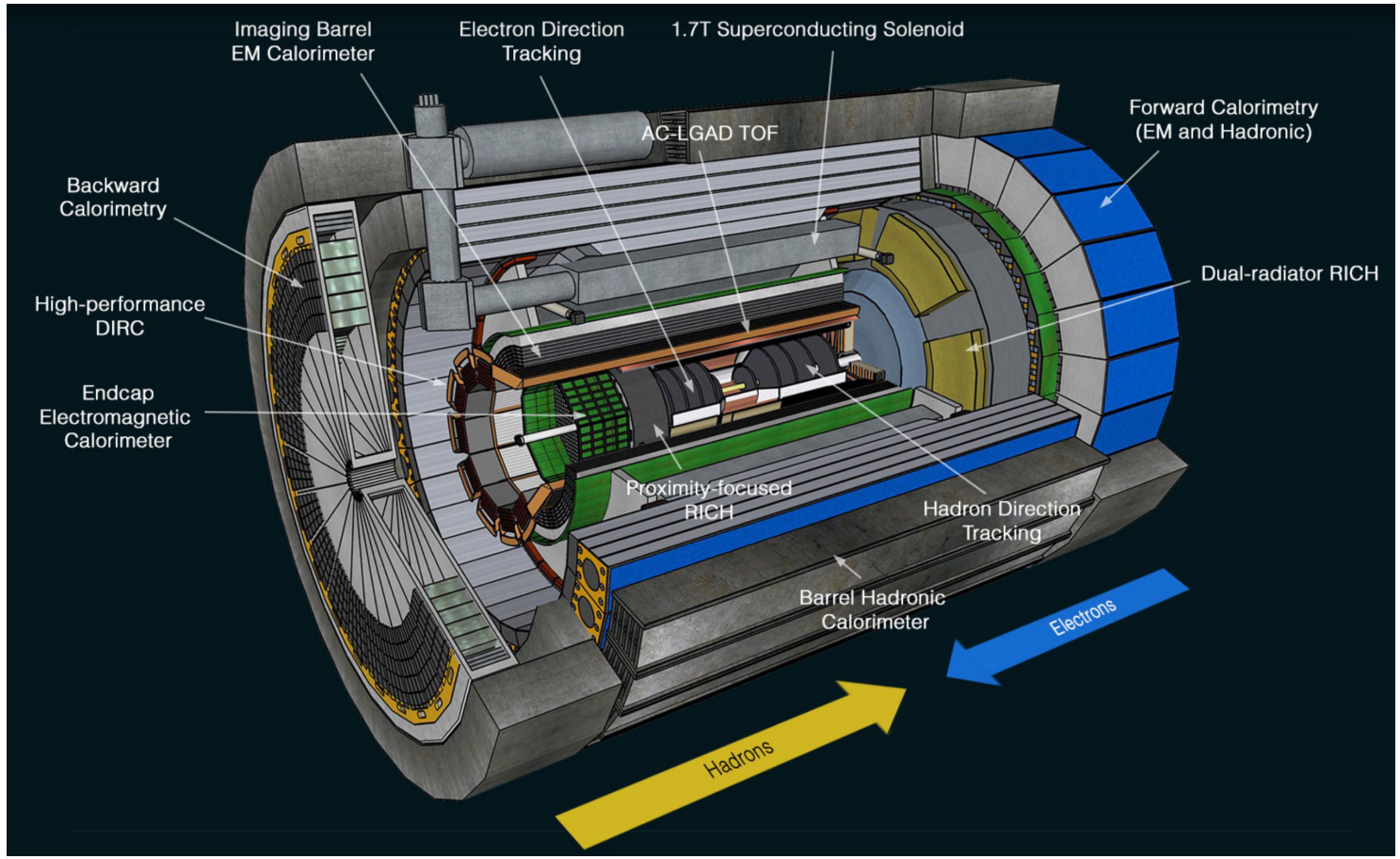


- Electron & proton beams with >70% polarization
- Ion beams, up to U
- Center-of-mass energy range √s ~ 20 – 140 GeV
- Luminosity 100 … 1000 times compared to HERA
  - up to 100 fb^{-1} / year

- Re-use one of the RHIC hadron rings
- Build a new general purpose detector in IP6



ePIC: EIC general purpose detector @ IP6



Tracking:

- New 1.7 T solenoid magnet
- Si MAPS Tracker
- MPGDs (μRWELL/μMegas)

PID:

- hpDIRC
- pfRICH
- dRICH
- AC-LGAD (~30ps TOF)

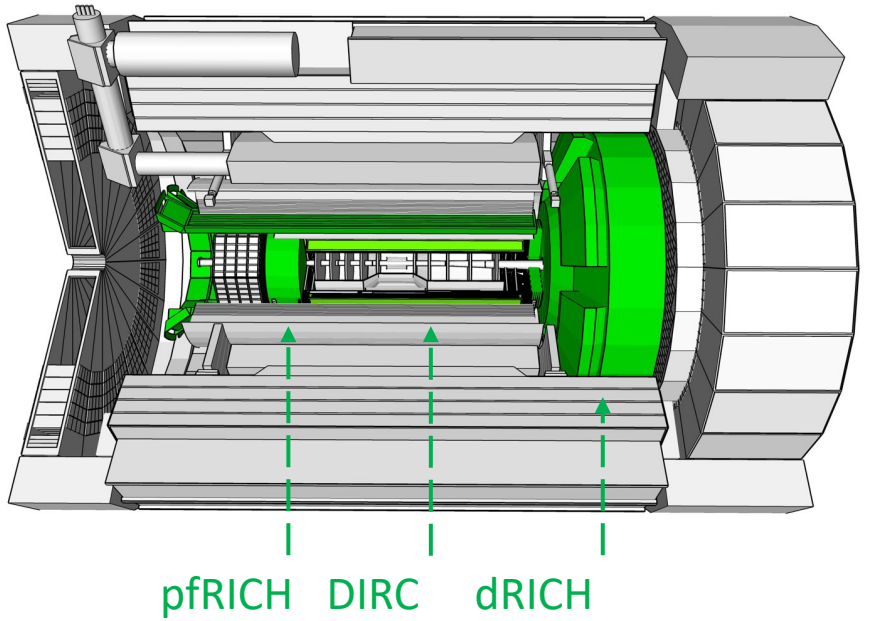
Calorimetry:

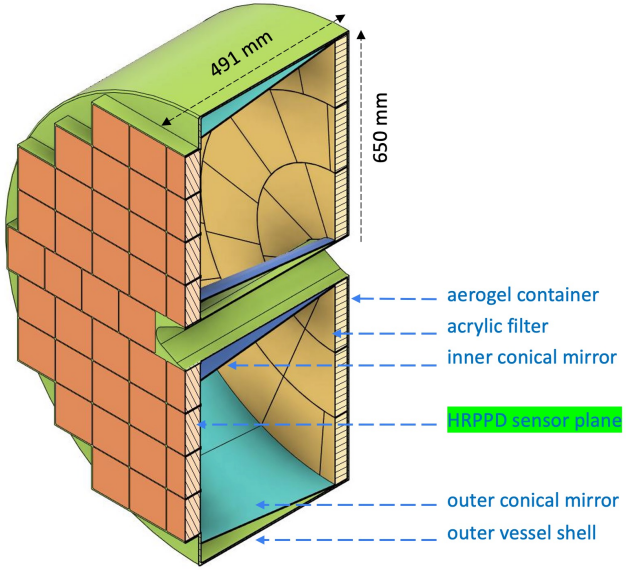
- Imaging Barrel EMCal
- PbWO4 EMCal in backward direction
- Finely segmented EMCal + HCal in forward direction
- Outer HCal (sPHENIX re-use)
- Backwards HCal (tail-catcher)

- A compact central detector with several subsystems
  - (Almost) hermetic coverage in tracking, calorimetry & PID $-3.5 < \eta < +3.5$

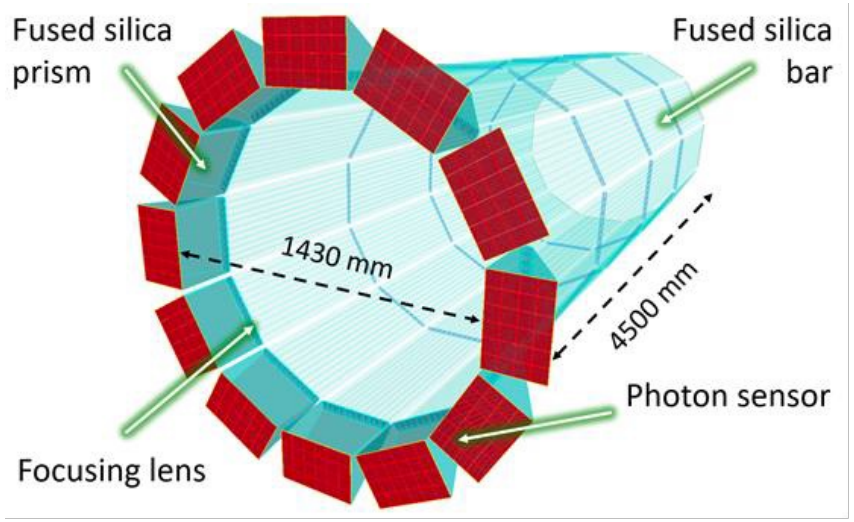
HRPPDs for EIC

- Backward RICH: low dark noise, ToF capability (vs SiPMs)
- DIRC: expected to be more cost-efficient (vs other MCP-PMTs)
- dRICH: problematic, because of the magnetic field orientation





pfRICH: 68 HRPPDs total

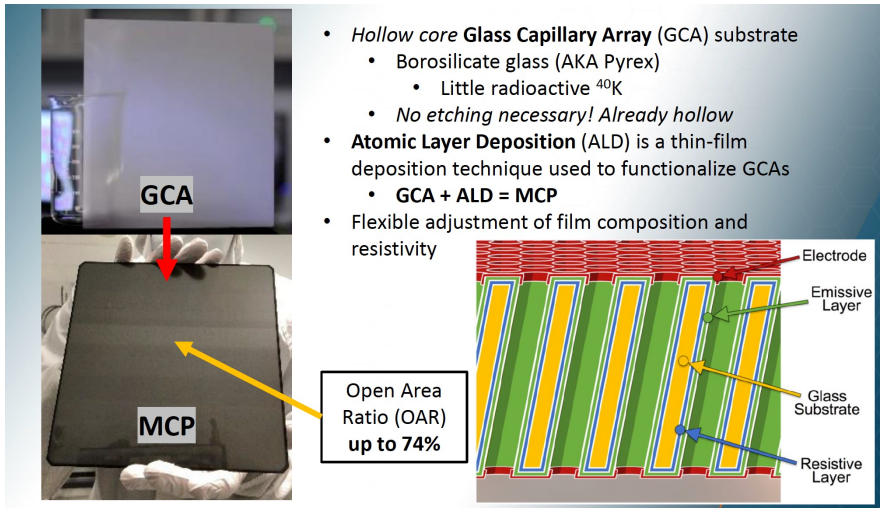


DIRC: 12*3*2 = 72 HRPPDs total

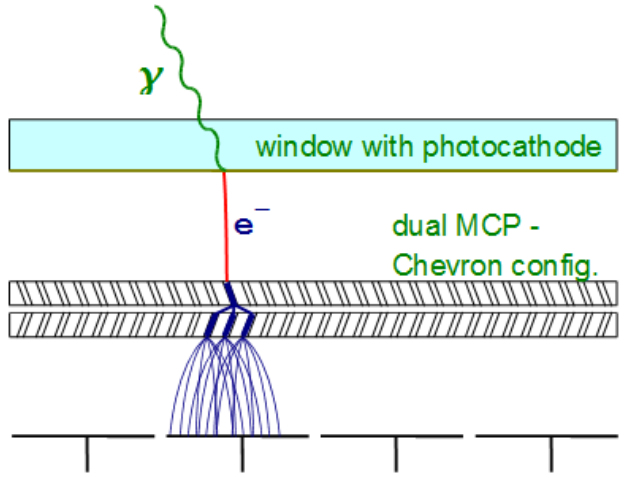
Focus so far was on the pfRICH application, where HRPPDs are a baseline photosensor choice

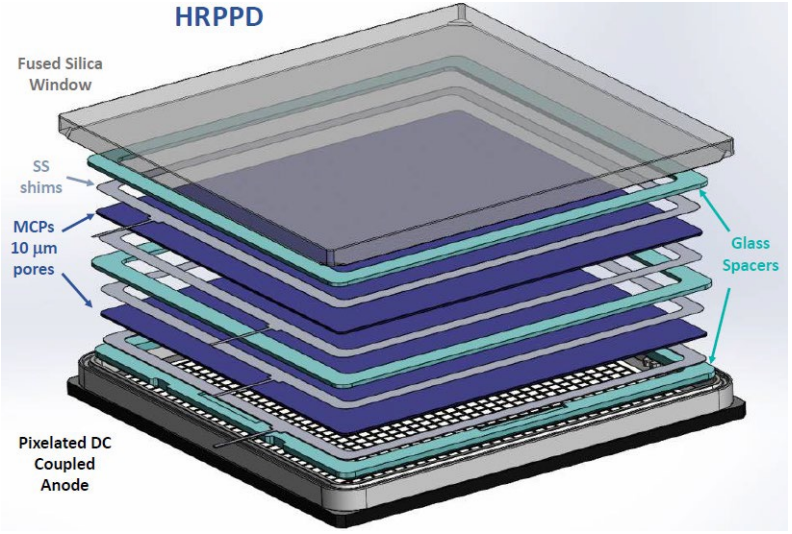
	pfRICH	DIRC
Spatial resolution	Sub-mm	Sub-mm
SPE timing resolution	σ of the core part <50ps	<75ps RMS, including tail
Dark count rate	Few kHz/cm^2 is acceptable	Few kHz/cm^2 is acceptable
Occupancy	Small: could work with large Gen II clusters	Large: require one SPE – one hit

Original HRPPD photosensors by Incom Inc.

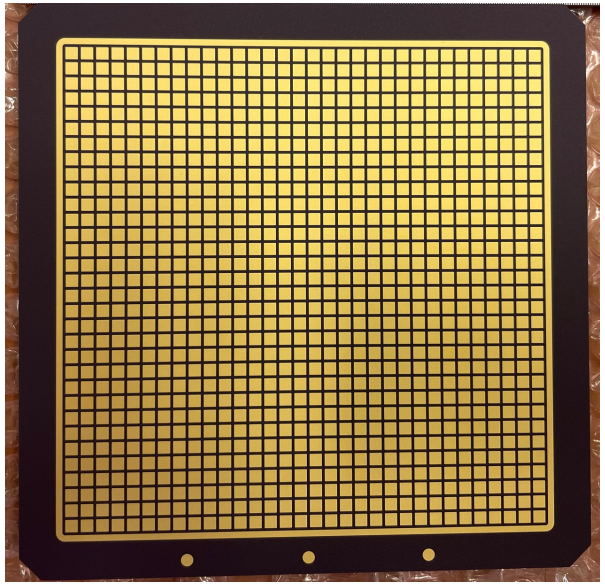


- *Hollow core* **Glass Capillary Array** (GCA) substrate
  - Borosilicate glass (AKA Pyrex)
    - Little radioactive ^{40}K
  - *No etching necessary! Already hollow*
- **Atomic Layer Deposition** (ALD) is a thin-film deposition technique used to functionalize GCAs
  - **GCA + ALD = MCP**
- Flexible adjustment of film composition and resistivity



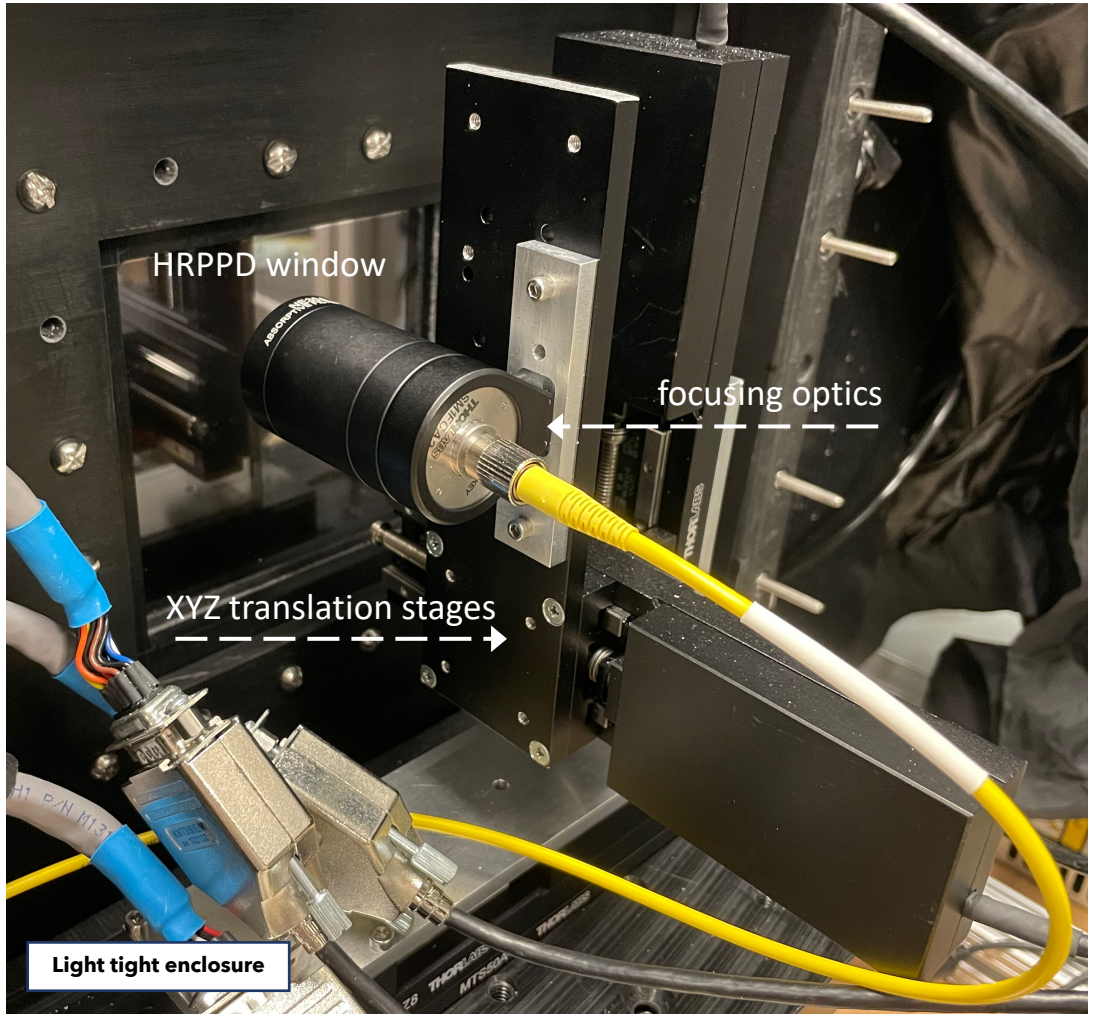


- An affordable large area vacuum photosensor
  - Up to ~3 times more cost efficient in $$ per mm^2 than other commercially available MCP-PMTs
- 10x10 cm^2 active area
- DC-coupled square pads
- Quantum efficiency above 30%
- SPE timing resolution ~50 ps level or higher

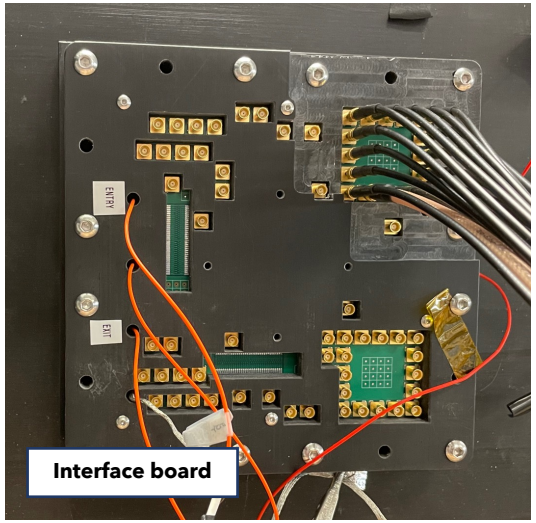


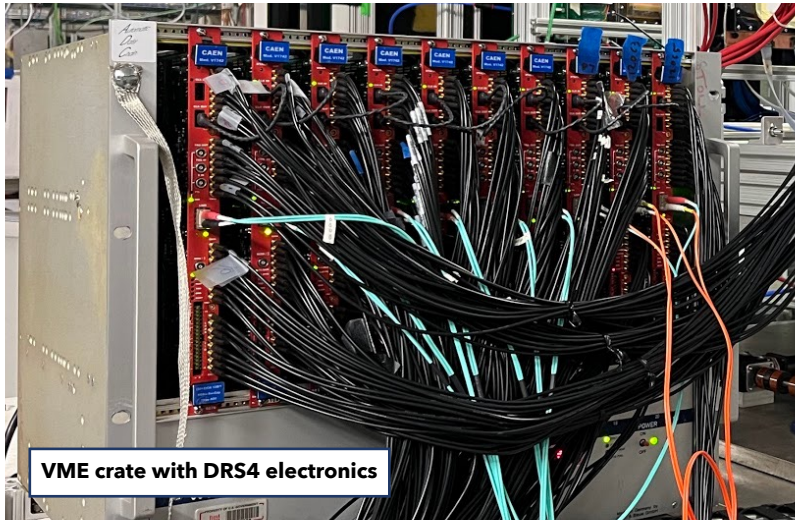
1024 ~3.2mm pads

HRPPD test stand at BNL



- Picosecond PiLas laser
- Compact light-tight enclosure
- 480 DRS4 channels (V1742 digitizers)
- Readout board with a pogo pin interface
  - MCX and high-density Samtec connector interface to DRS4



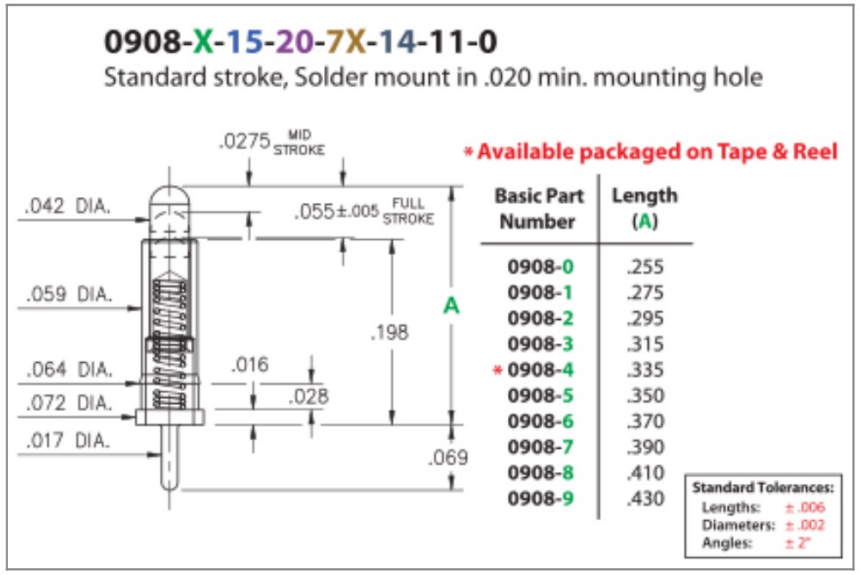


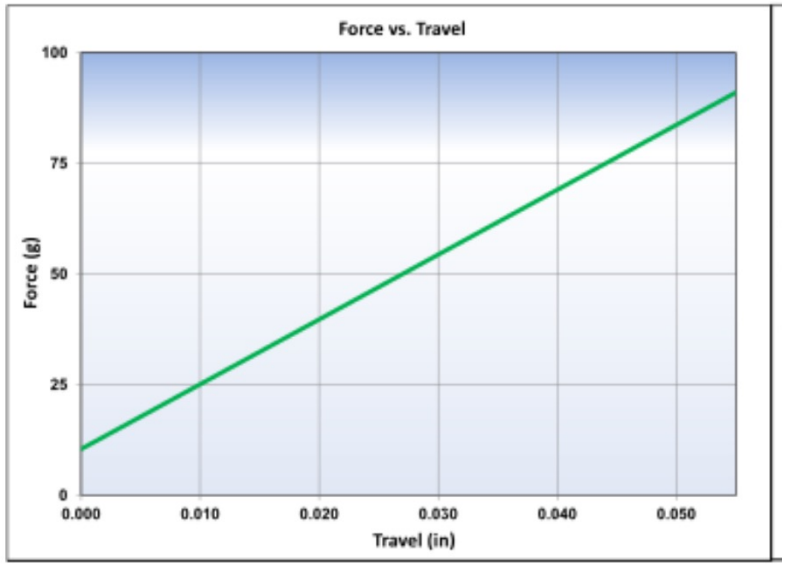
Similar setups exist at Argonne, INFN Trieste & Glasgow, though they are oriented on capacitively coupled LAPPDs, and typically, have up to 32 (64) channels of DRS4 electronics

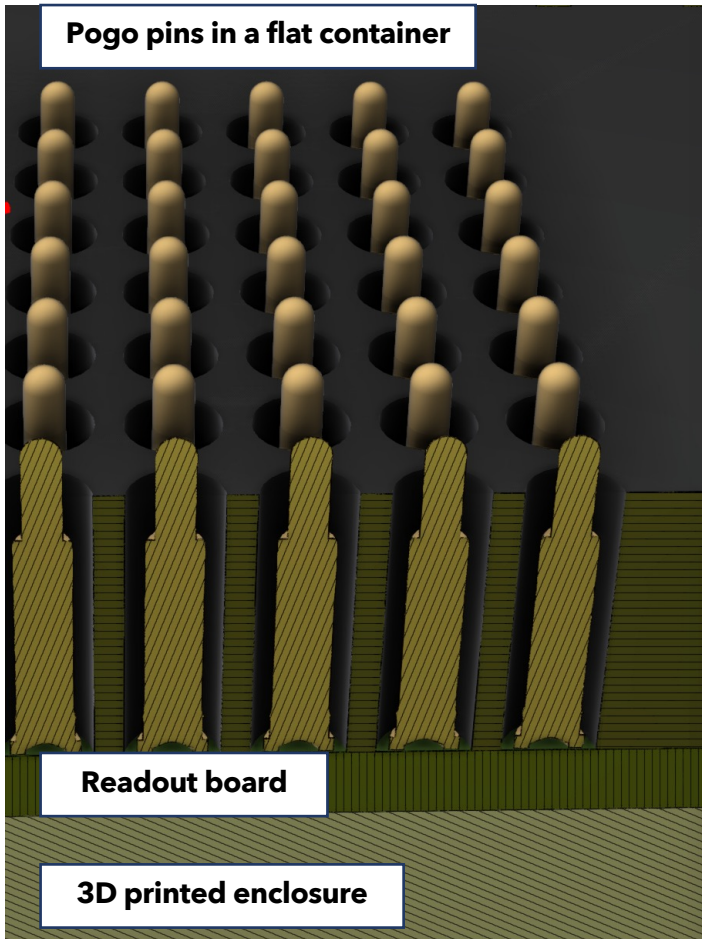
Integration attempt #1: pogo pins

Signal pogo pins: Mill Max 0908 series

#72 SPRING LOW FORCE SPRING	Full Stroke Capability : .055"± .005" [1,4 ± 0,127]
Spring Material : Beryllium Copper Alloy 172	Force @ Mid. Stroke : 45 g ± 20 g
Mid. Stroke : .0275" [0,7]	Initial Force (Pre-Load) : 15 g

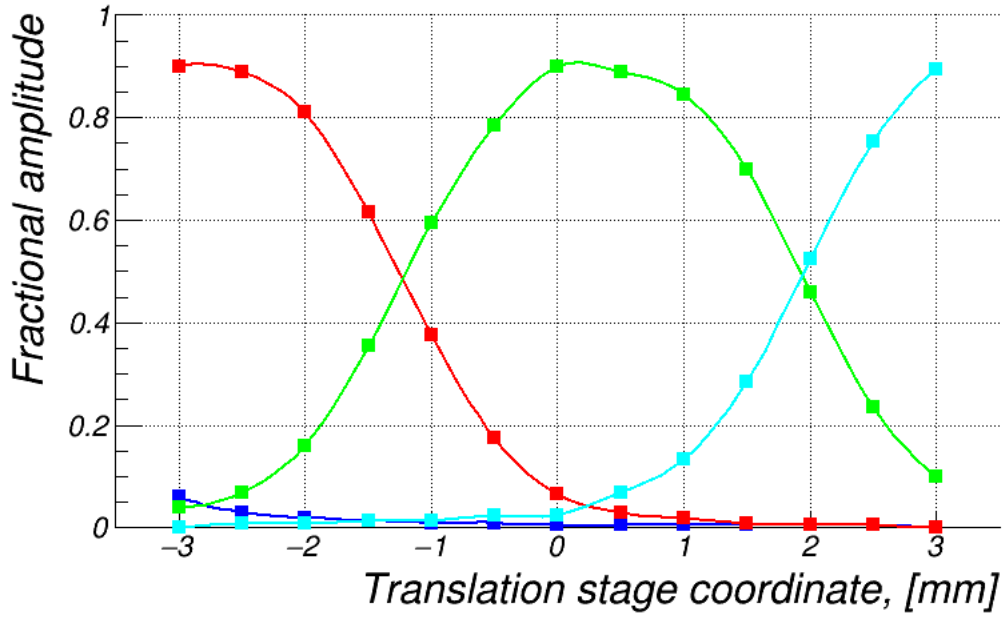


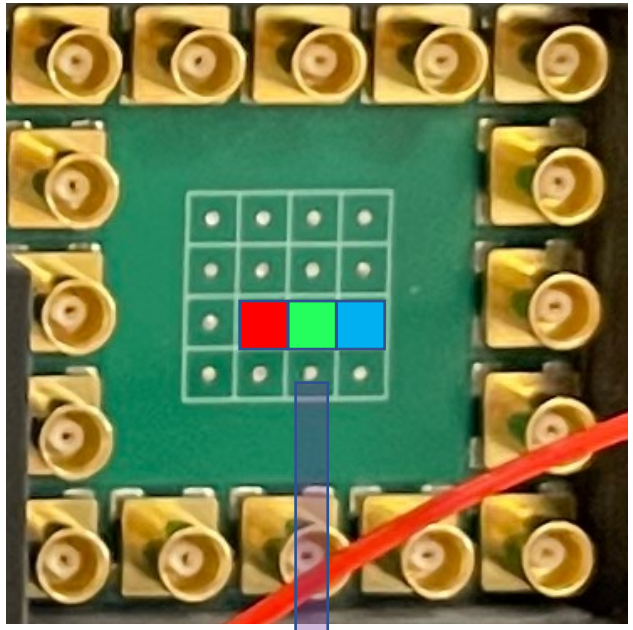




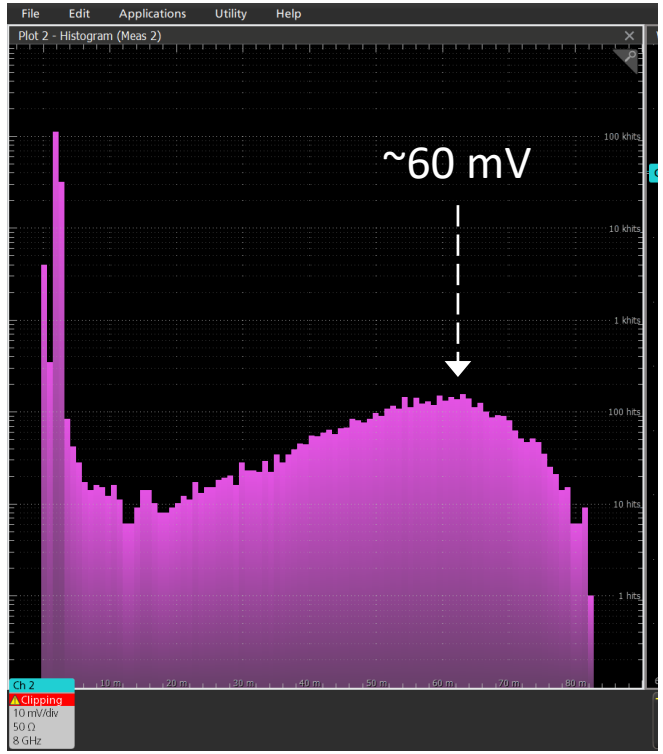
- Should suffice for a basic performance evaluation

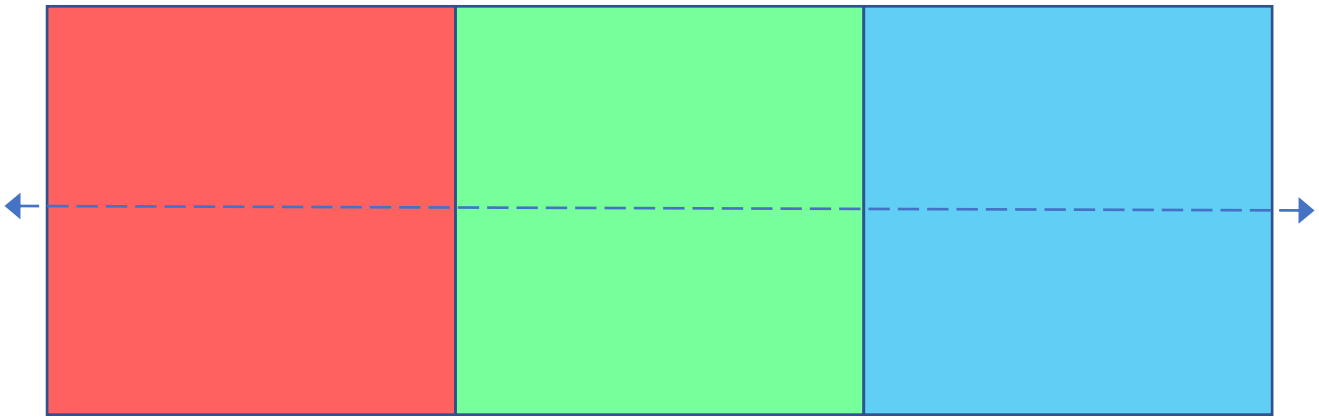
HRPPD #6: charge sharing





Amplitude spectrum on a scope

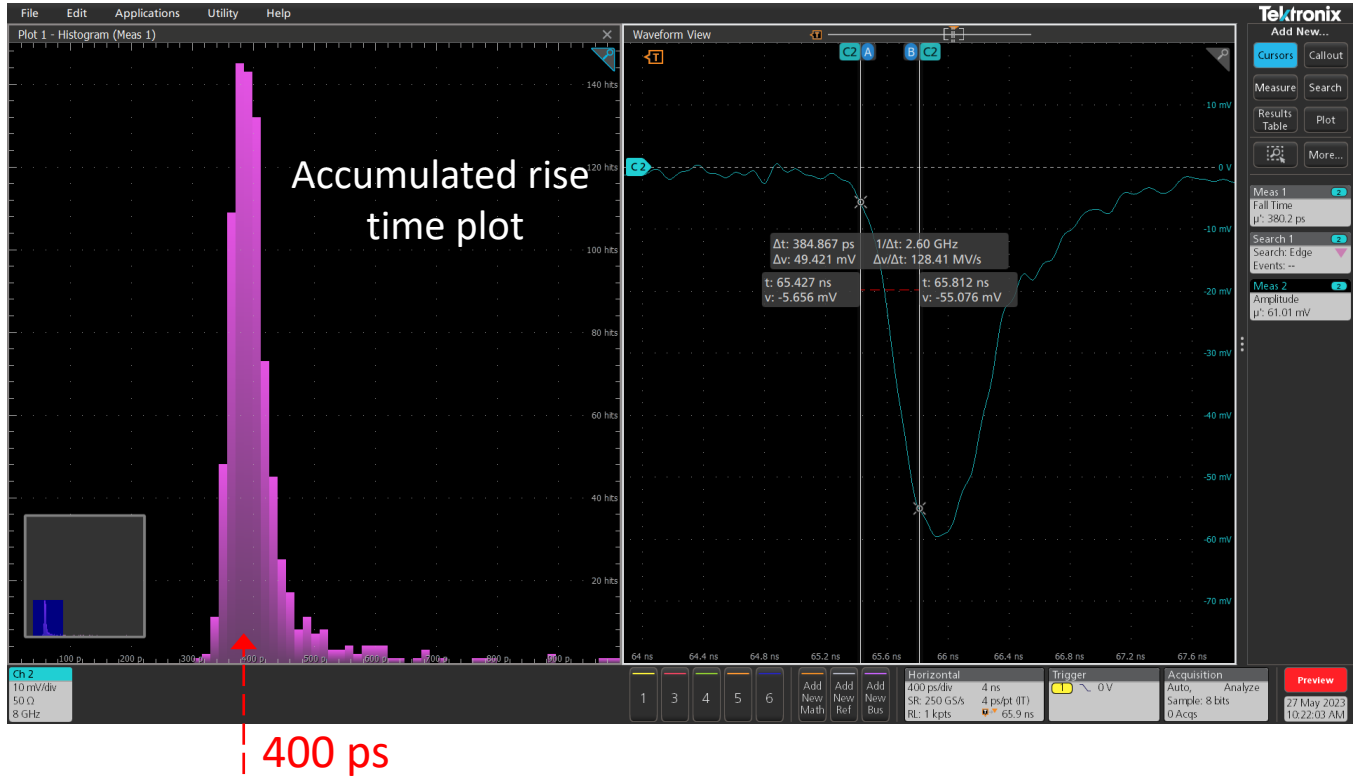




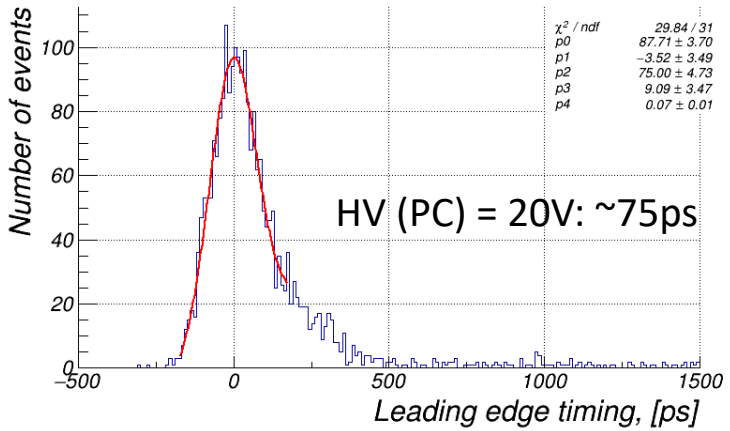
amplitude scan across three neighbor pads

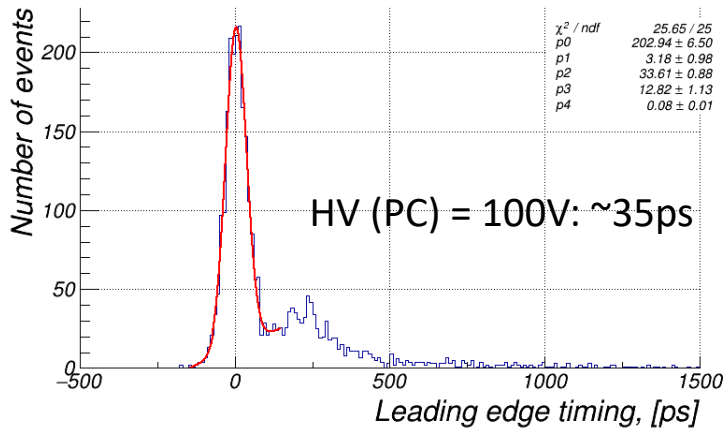
- Moderate charge sharing (even without a B field)
- Expect ~3.2mm/√12 spatial resolution or better

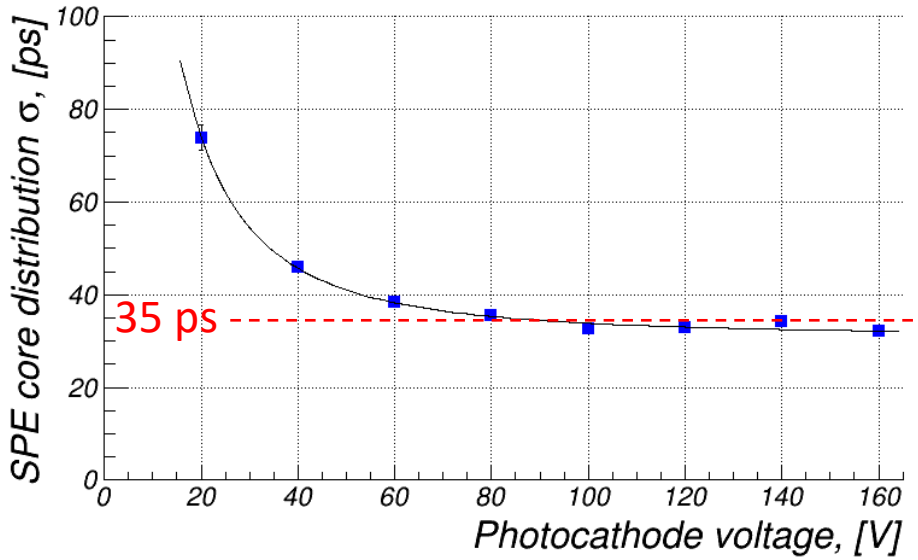
HRPPD #6: timing performance with a 420nm laser



- Laser focused to a pad center
- Intensity tuned down to ~95% empty events
- Δt data taken with a V1742 DRS4 module
  - Channel #0 – HRPPD pulse
  - Channel #1 – laser synchro pulse
- *Neither laser pulse width nor other instrumental effects unfolded*

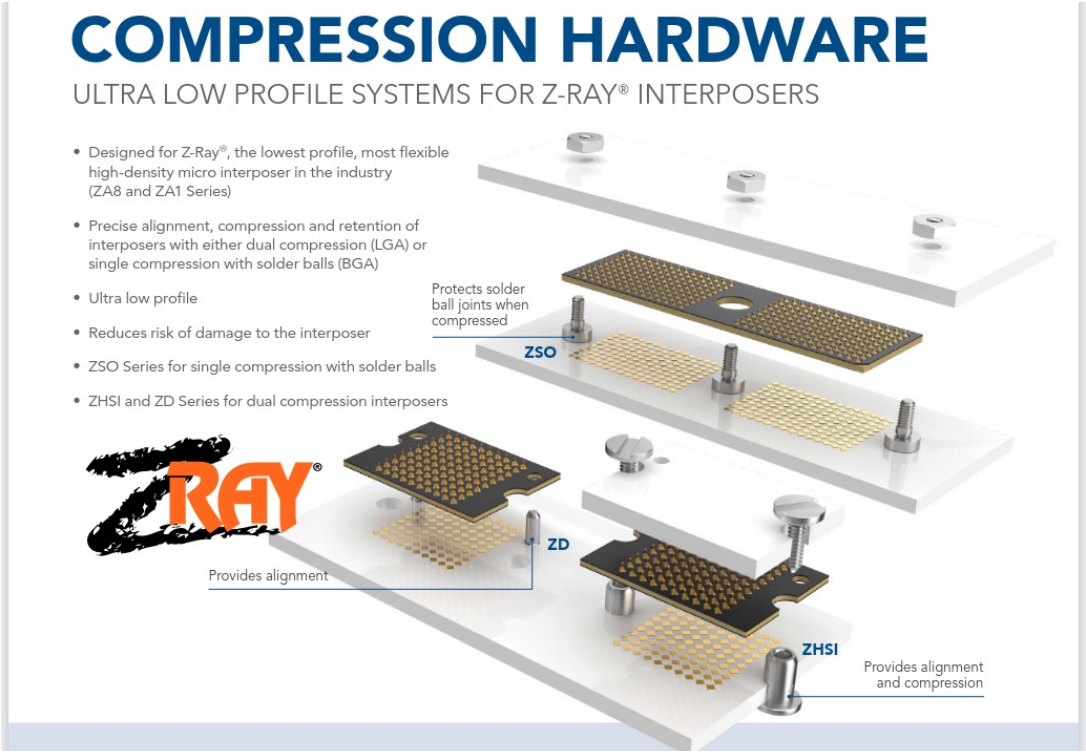


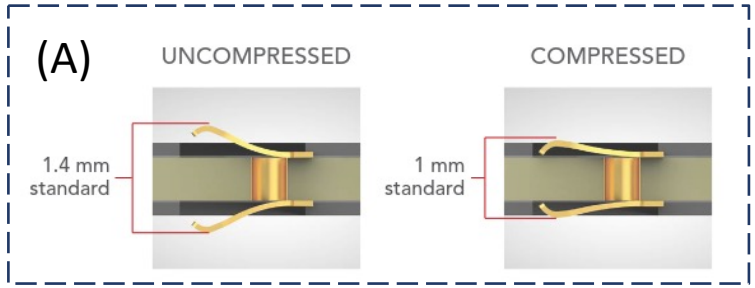


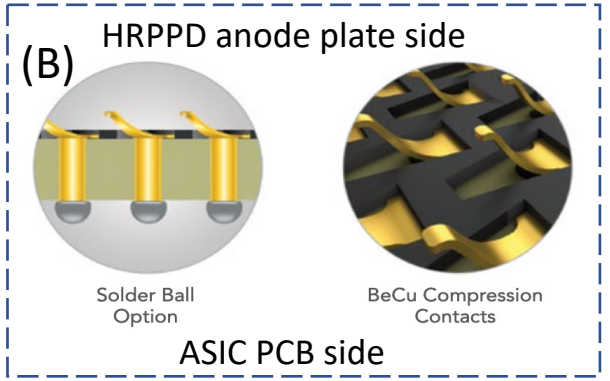


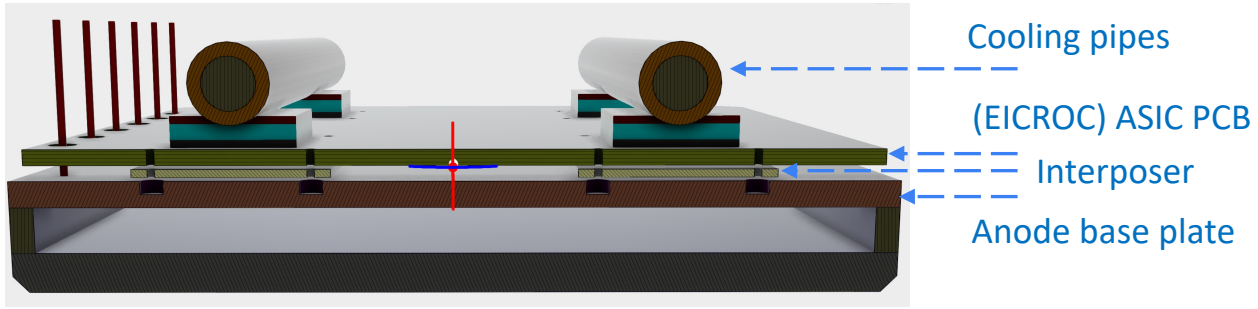
Integration attempt #2: compression interposers

- Design custom LTCC anode base plates for new EIC HRPPDs
  - Samtec compression interposers look like a reasonable interconnect option
  - Fallback solution: conductive epoxy screen printing





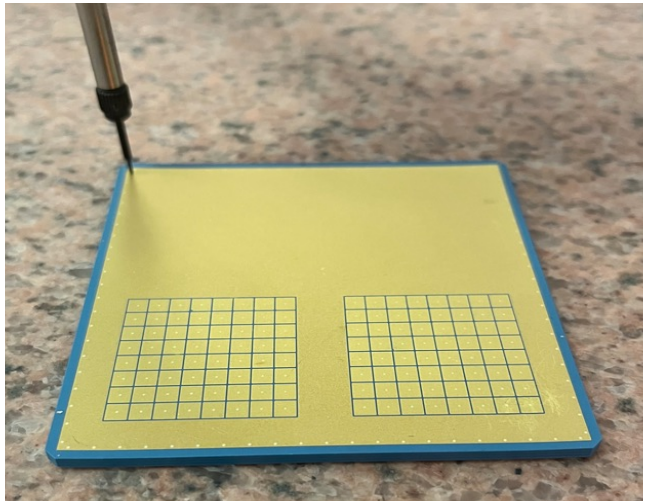


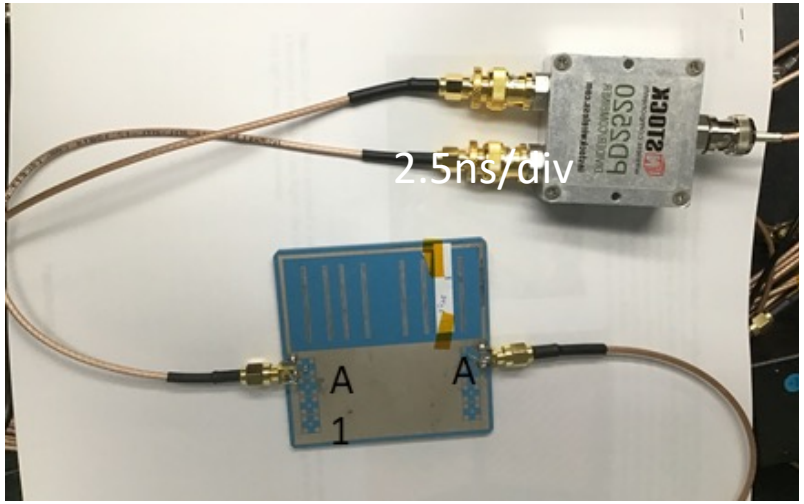


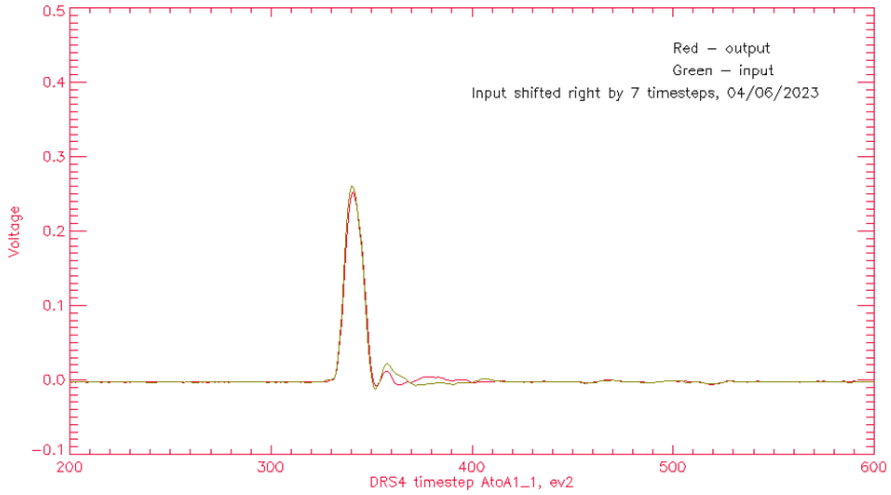
HRPPD face down

Small size LTCC prototypes by Techtra (Poland)

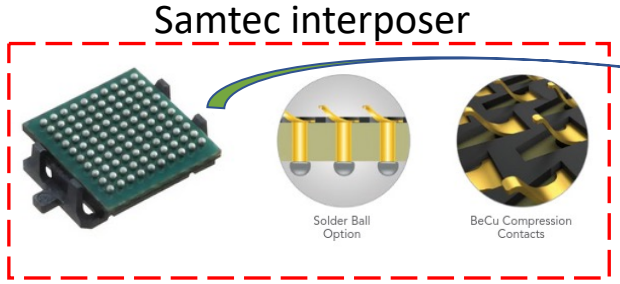
- First two 3” LTCC anode plates were examined at Incom
  - Flatness and vacuum tightness look fine
  - No measurable cross-talk introduced in the ceramic stack
    - 50 Ohm impedance matched isolated coplanar waveguide trace configuration
  - Small trace capacitance (<2pF/cm) confirmed
  - Signal degradation confirmed to be marginal, and only on very long (6cm) traces

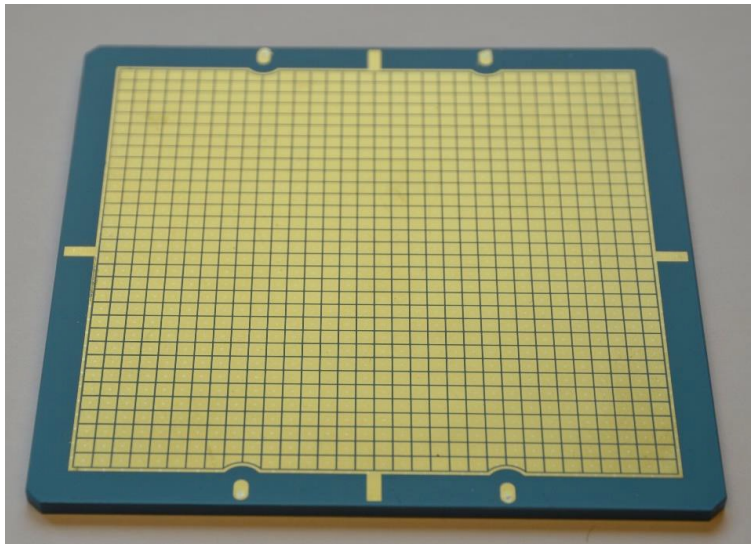




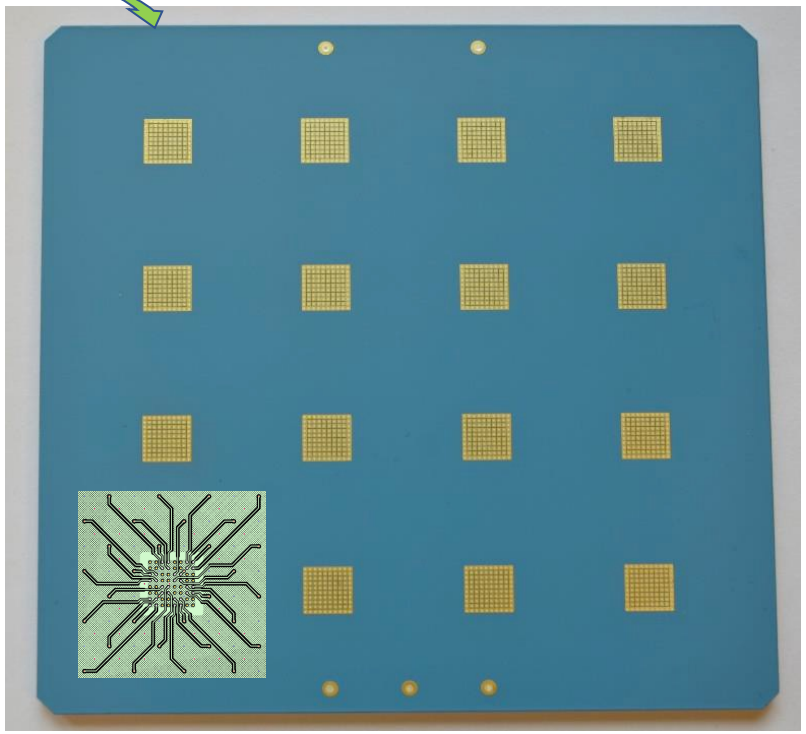


Full size prototype by Techtra (Poland)

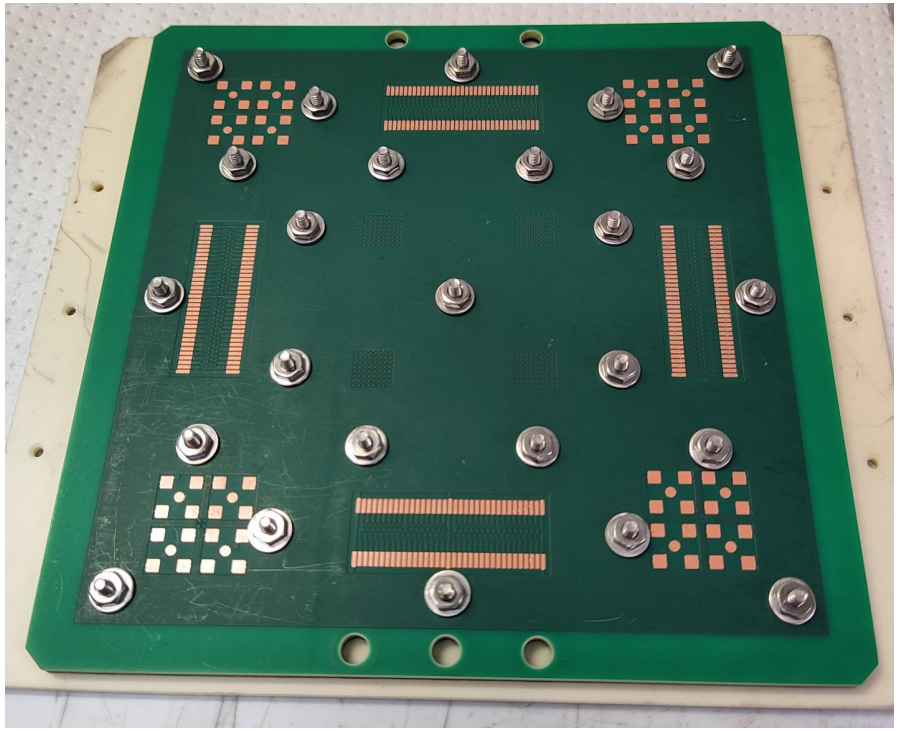




Inner side of a 32x32 pad ceramic 120mm base plate



Outer side with 4x4 800 μm pitch 64-pixel fields & a routing snapshot

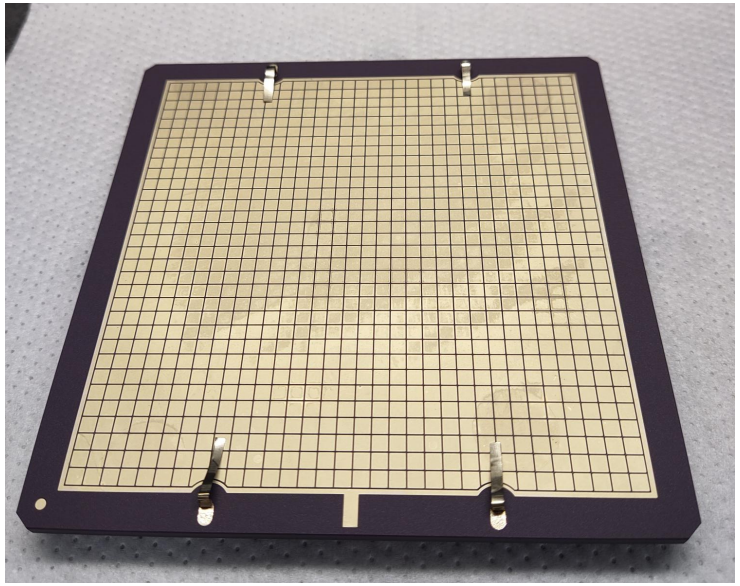


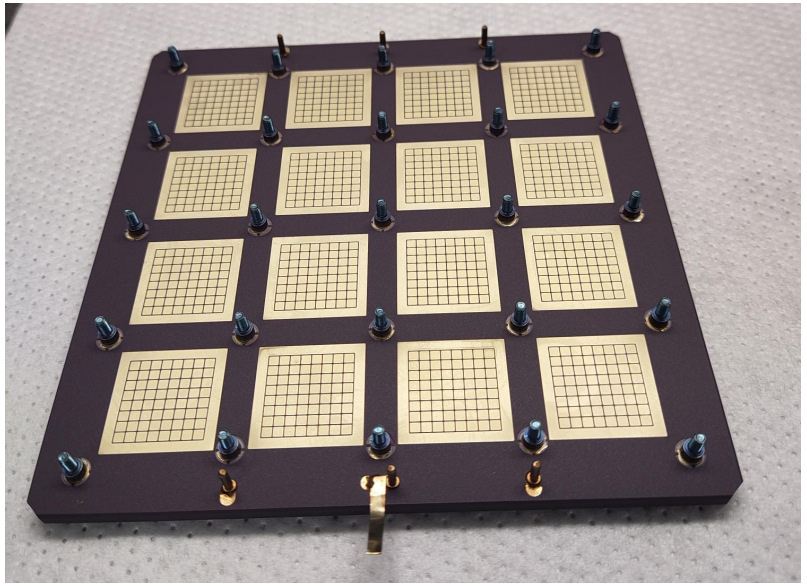
A “simple connectivity” PCB (Samtec interposers on the front side & MCX + high density connectors on the rear side)

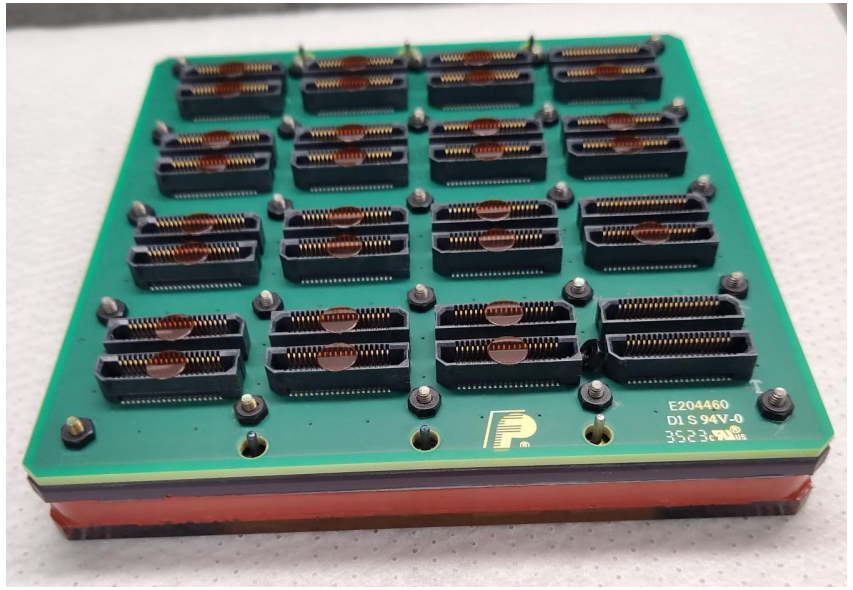
- Looked fine, was flat enough and vacuum tight
  - However, ~10% of pads shortened to ground
  - We were not able to build a functional HRPPD tile

The first five EIC HRPPD anodes were at the end ordered from Kyocera (Japan)

EIC HRPPDs



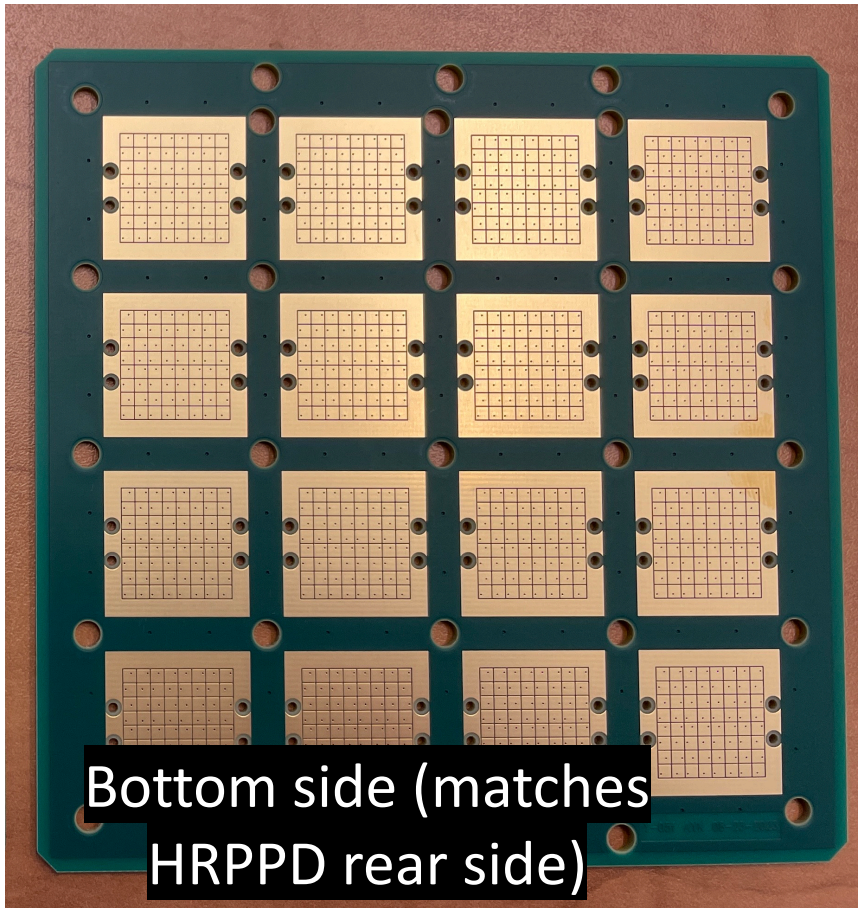


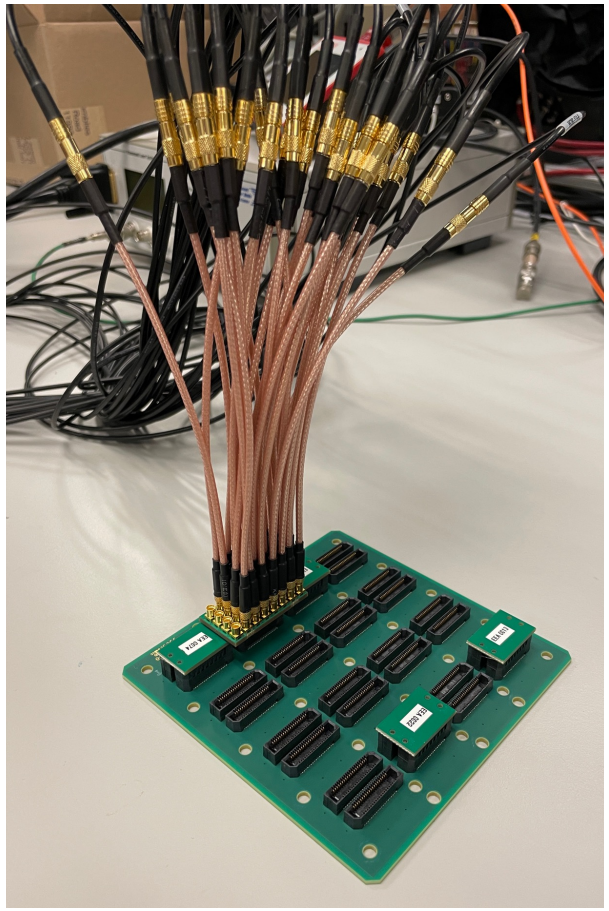


- June 2023: a “staged” EIC / Incom Project Engineering Design (PED) contract:
  - Phase I: finalize remaining R&D to the extent needed (by September 2023)
    - Anode design similar to the second (full size) iteration with Techtra (75% geometric efficiency)
    - A more relaxed 2mm pitch custom Samtec compression interposer design
  - Phase II: procure 5 HRPPDs (September - February 2023)

  - “Phase III”: perform bench tests and beam test evaluation well ahead of the EIC CD-2 review

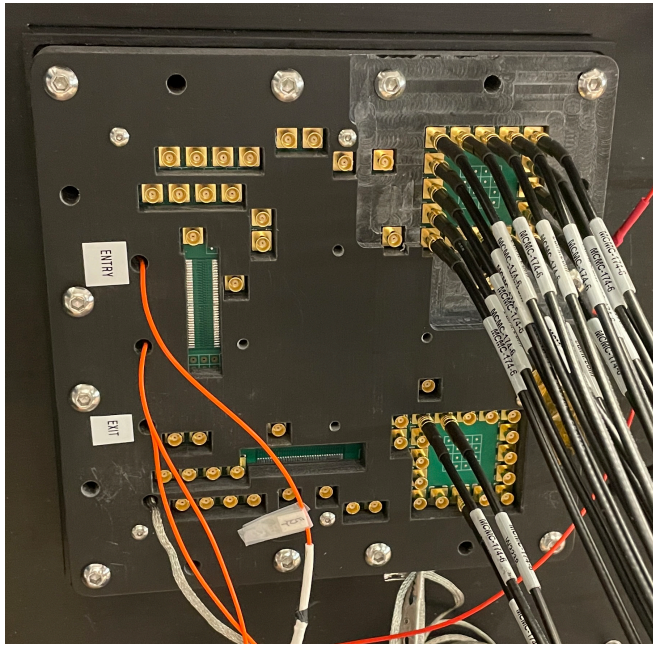
EIC HRPPD passive interface #1

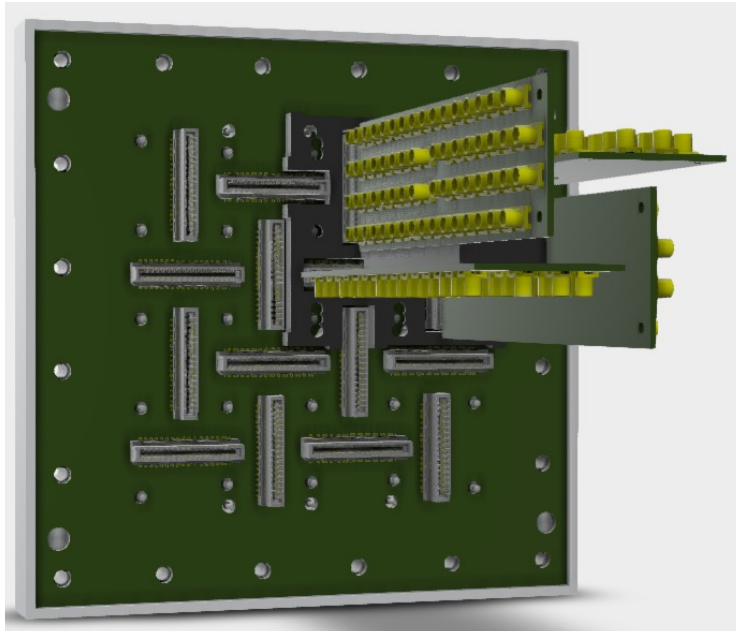


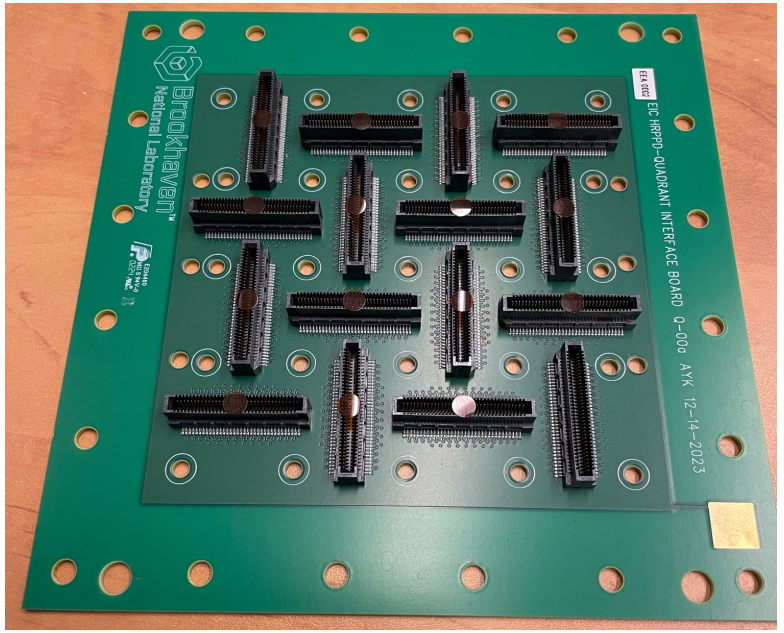


- For installations with a low electronics channel count
- Samtec -> MMCX adapter; MMCX -> MCX pigtail cables, grounding caps
- Four sets assembled by now (one @ JLab, one @ Incom)

EIC HRPPD passive interface #2

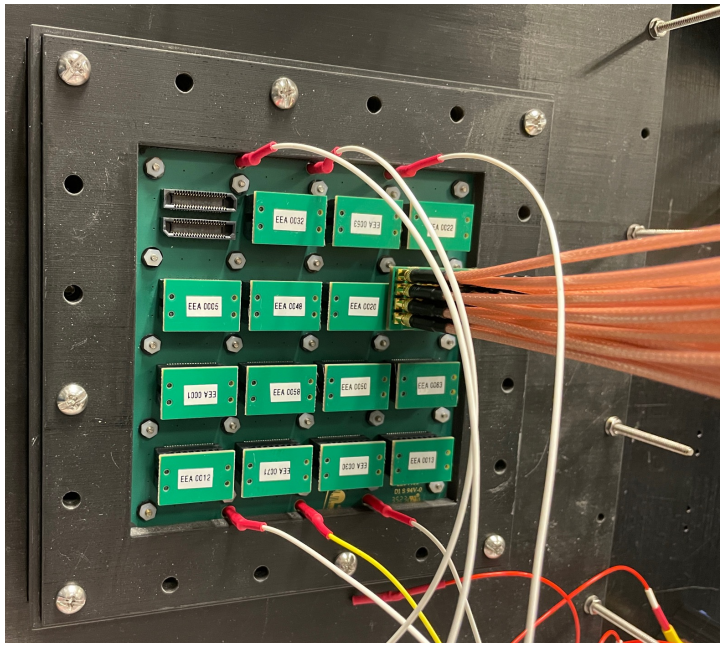


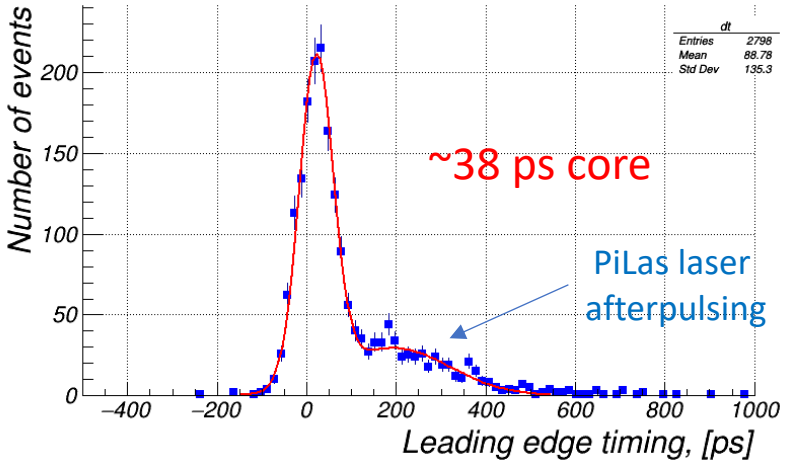




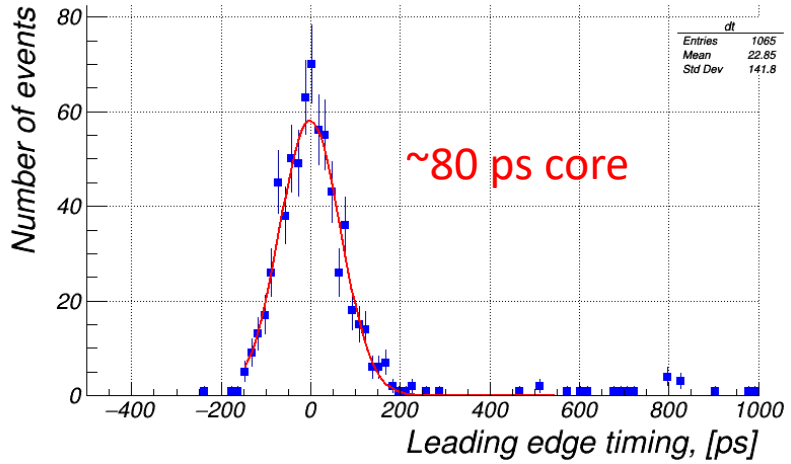
- Interface to the existing 64-channel edge-to-MCX adapter cards
- Allows one to scan a full HRPPD quadrant at once (256 channels)
- Two sets assembled (one @ Incom & one @ BNL)

HRPPD #15: timing performance with a 420nm laser



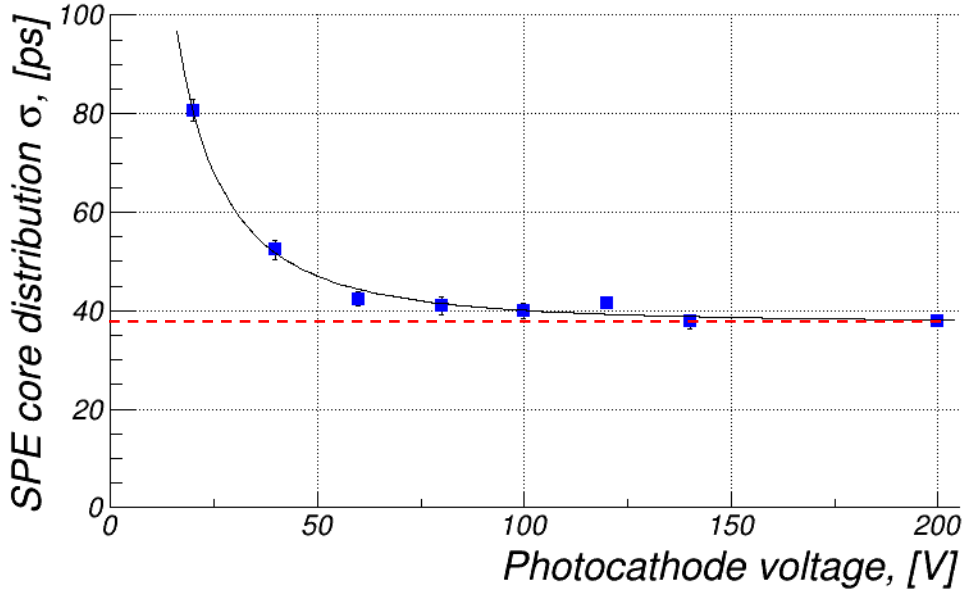


0% laser tune, 200V on photocathode



25% laser tune, 20V on photocathode

- Laser focused to a pad center
- Intensity tuned down to >99% empty events
- Δt data taken with a V1742 DRS4 module
  - Channel #0 – HRPPD pulse
  - Channel #1 – laser synchro pulse
- *Neither laser pulse width nor other instrumental effects unfolded*



ASIC considerations

- **A standard requirement list**
  - Provide timing resolution <20ps and amplitude measurement
  - Work with collected charge from few dozens to few hundred fC
  - Work with a relatively high detector capacitance up to 10 pF
  - Have high channel density (64 channels per ASIC and more) and few mW/ch power dissipation
  - Streaming mode (either this or that way)

Waveform digitizer (e.g. by Nalu Scientific)

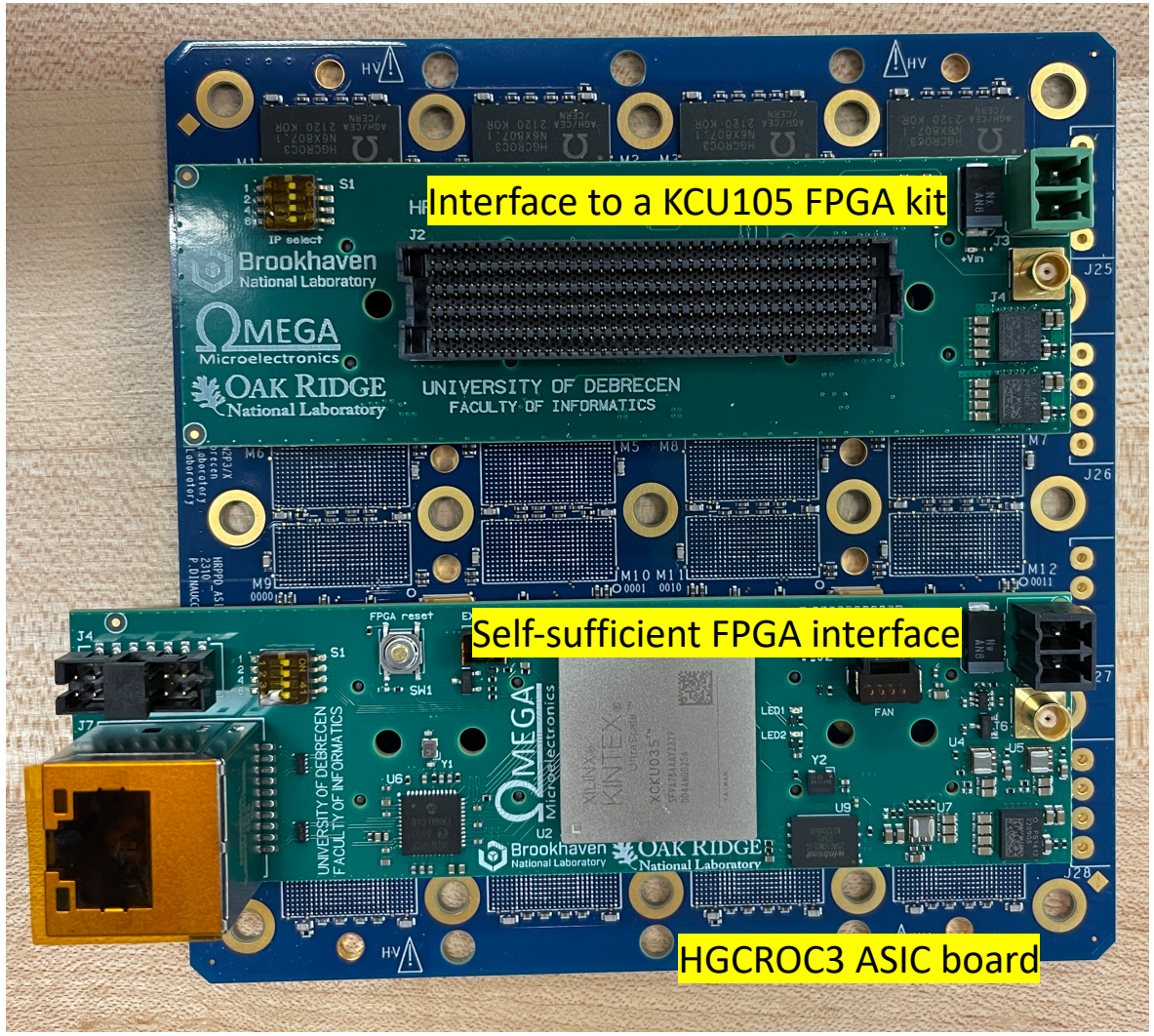
- Pros
  - Expect higher timing resolution overall
  - Performance less affected by signal shape
- Cons
  - Higher expected power dissipation
  - Not readily available with a high enough channel count

TOA/ADC (EICROC by OMEGA group)

- Pros
  - Supported by the EIC project
  - HGCROC3 is available as a starting point
  - Expected power dissipation ~1-3mW/ch
  - Should work with HRPPDs at a lower gain
- Cons
  - Assumes signals have a “regular” shape

HRPPD HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA], Uni Debrecen, BNL, Oak Ridge



- V0 iteration is ~complete
  - Four partly staffed ASIC boards
  - Few passive interface boards (for use with a KCU105 kit)
  - One FPGA board
  - Cooling stuff (heat sinks, fans) for five HRPPDs
- Passive interface debugging takes more time
  - Host PC -> FPGA -> ASIC connectivity is established
- Current effort & next steps:
  - Debug the driver using FMC+KCU105 configuration
  - **Make sure HRPPDs work with this analog frontend**
  - Verify that FPGA-based implementation works
  - Proceed with ordering V1 backplane sets for 5-7 HRPPDs

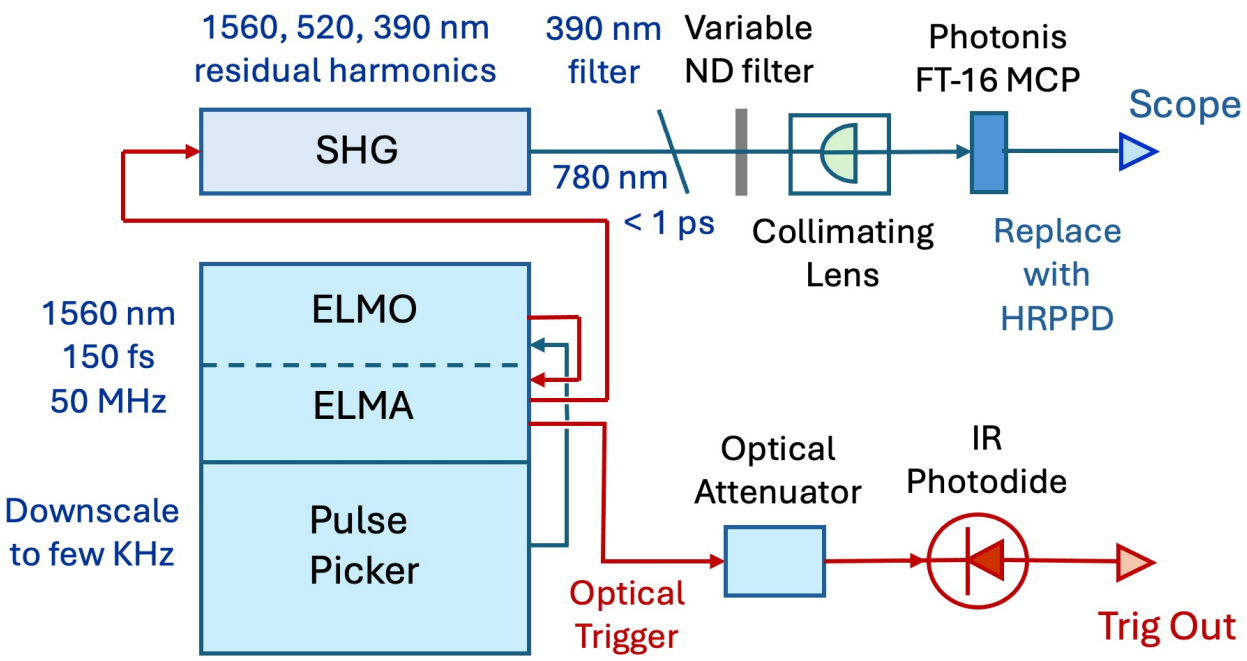
Femtosecond laser calibration system @ BNL

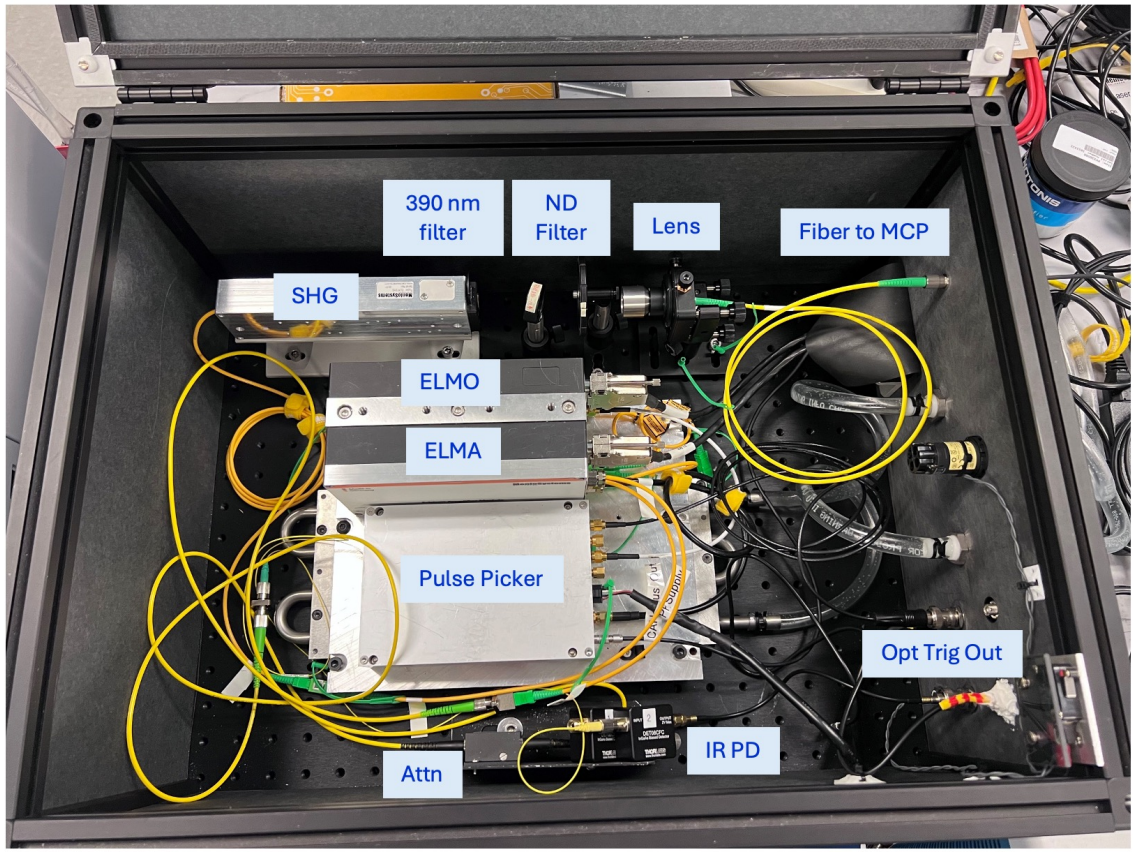
Menlo Systems Elmo 780 Erbium Fiber Femtosecond Laser

ELMO = Primary Laser Oscillator

ELMA = Optical Amplifier

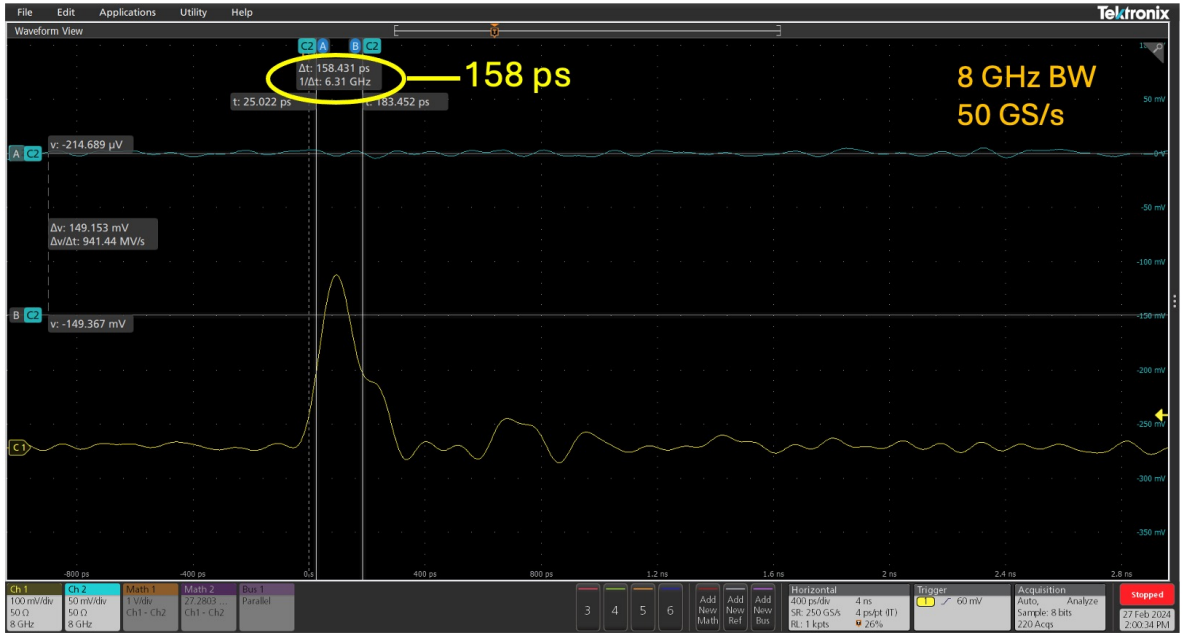
SHG = 2nd Harmonic Generator



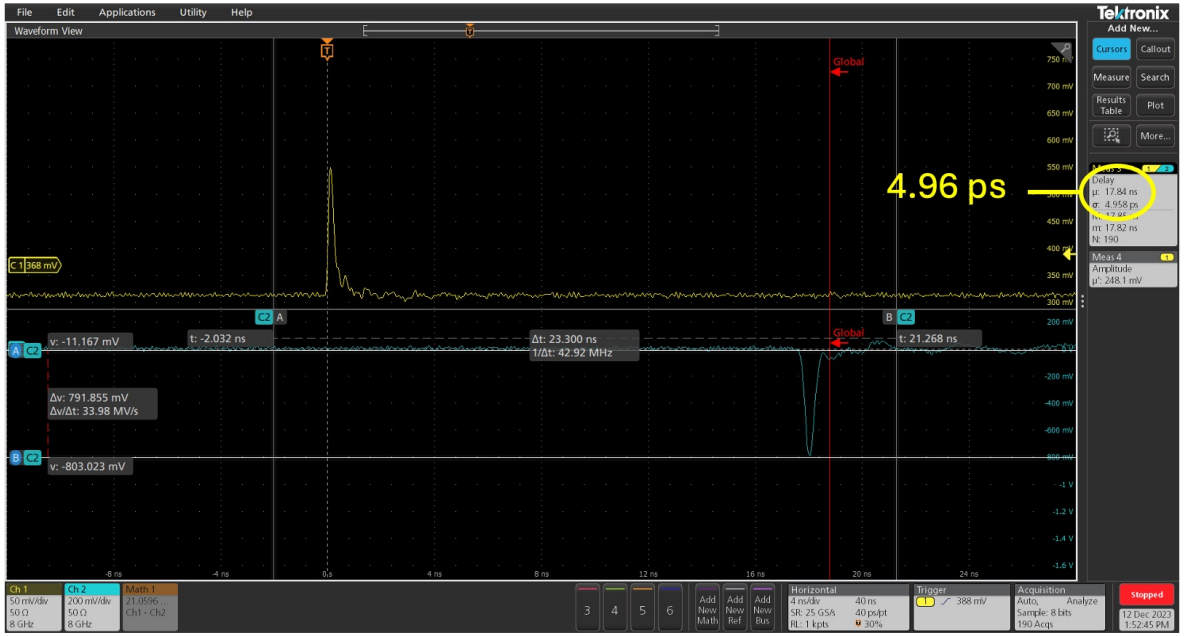


Measurements with Photonis MCP-PMT

IR Photodiode Pulse
Rise Time ~ 70 ps
Pulse Width < 160 ps



Time Jitter between Photodiode Trigger and MCP < 5 ps



Conclusion: we should be able to make timing measurements with a resolution < 10 ps

EIC HRPPD evaluation procedure

- Primary QA at JLab (see Arshak's talk)
- More systematic active area scans (including ps timing) at BNL

- Magnetic field resilience studies at Argonne in late summer 2024
  - Parasitic to MCP-PMT evaluation
  - Staffed by Argonne, BNL, JLab, USC
  - Main objective: gain and timing performance recovery in a "typical" pfRICH and hpDIRC B-field

- Photocathode ageing studies by INFN (see Jinky's talk)
- Side by side Photek Auratek & Incom HRPPD comparison in Glasgow
- Work on HRPPD HGCROC3 ASIC backplane (Debrecen / Brookhaven)
- Setting up a Brookhaven test stand clone at Yale

Summary & outlook

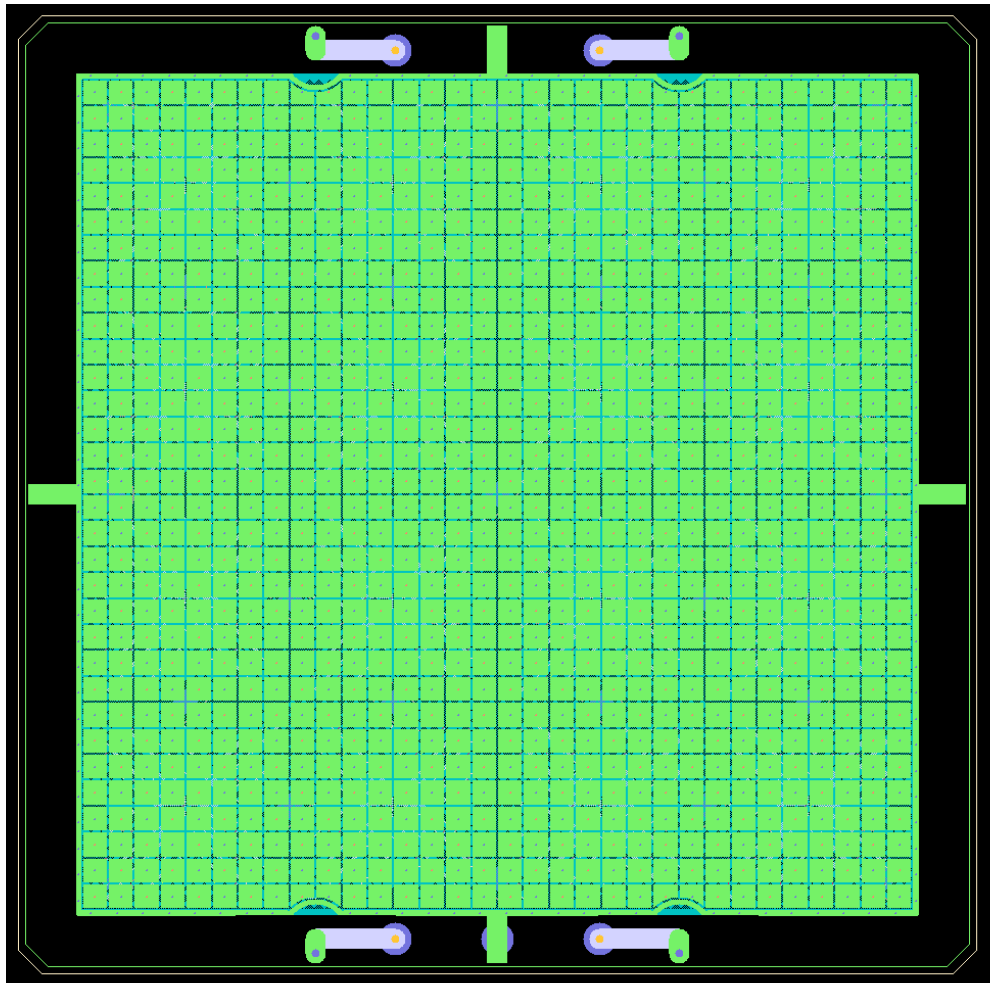
- Incom HRPPDs were adopted as ePIC EIC pfRICH baseline photosensor
- An EIC PED contract to re-design them and procure a small batch is pretty much complete
- 5+2 HRPPDs were ordered and delivered to JLab
  - The extra two are for hpDIRC evaluation

- Evaluation effort is ramping up in several EIC institutions around the world
- Work on ASIC backplane is in progress

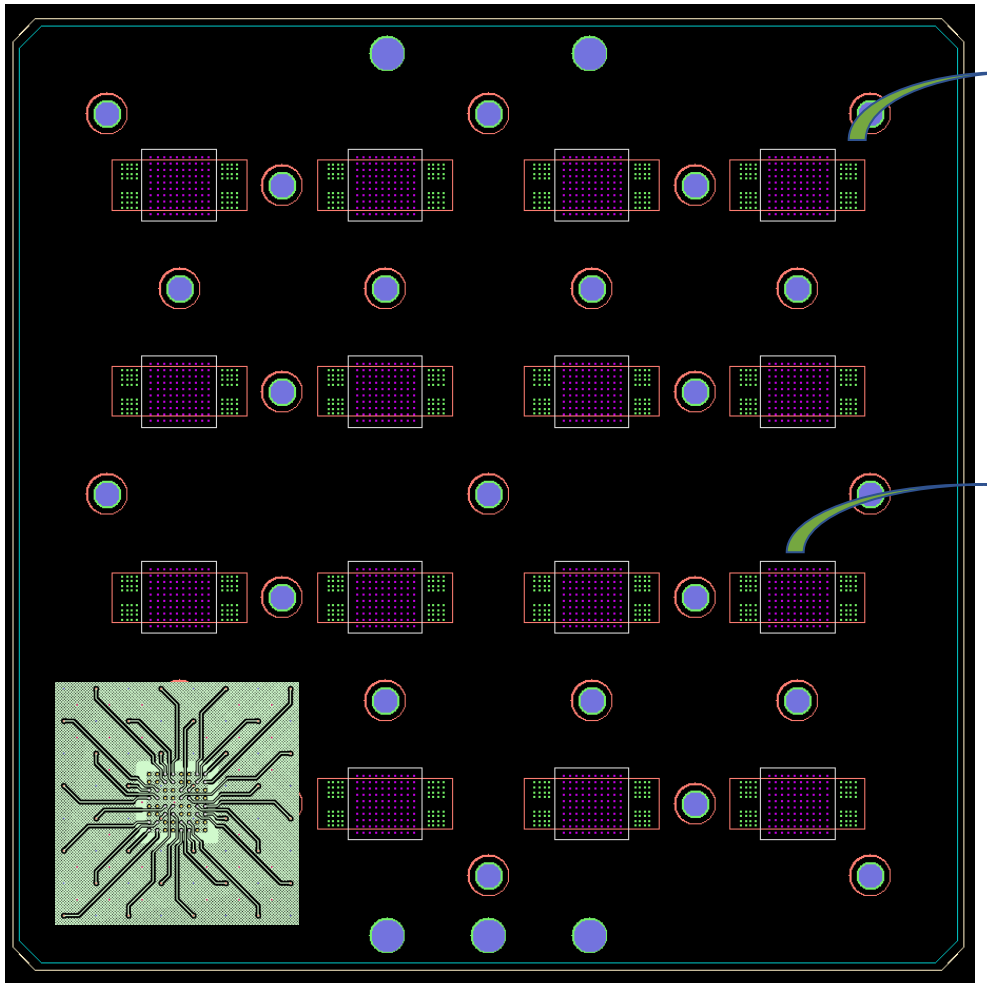
- Further plans will depend on the evaluation outcome by the end of summer 2024

Backup

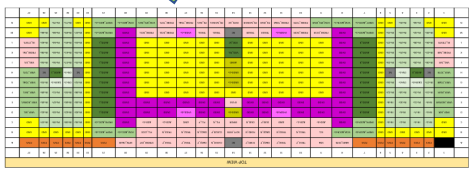
Full size anode base plate and a matching PCB



Inner side of a 32x32 pad ceramic base plate

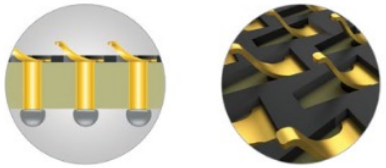


Outer side overlaid with a 16x HGCROC PCB template



HGCROC ASIC

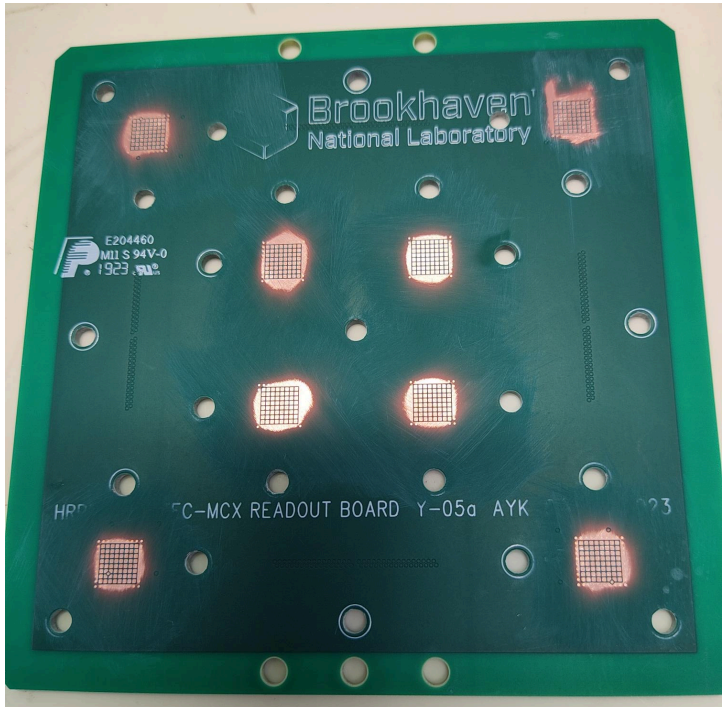
Samtec interposer



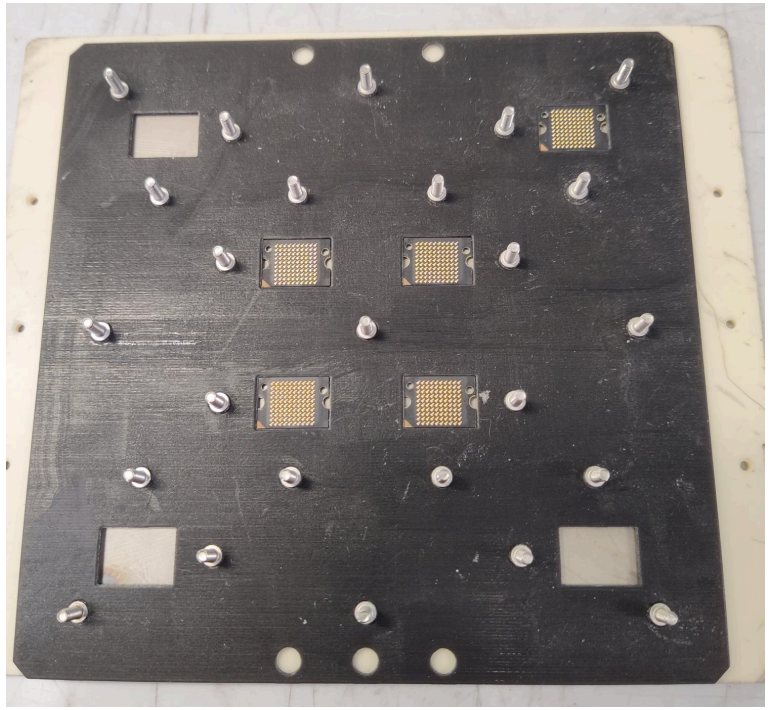
- This 120mm x 120mm LTCC base plate is now being built by Techtra

First iteration: a matching Y05a connector board

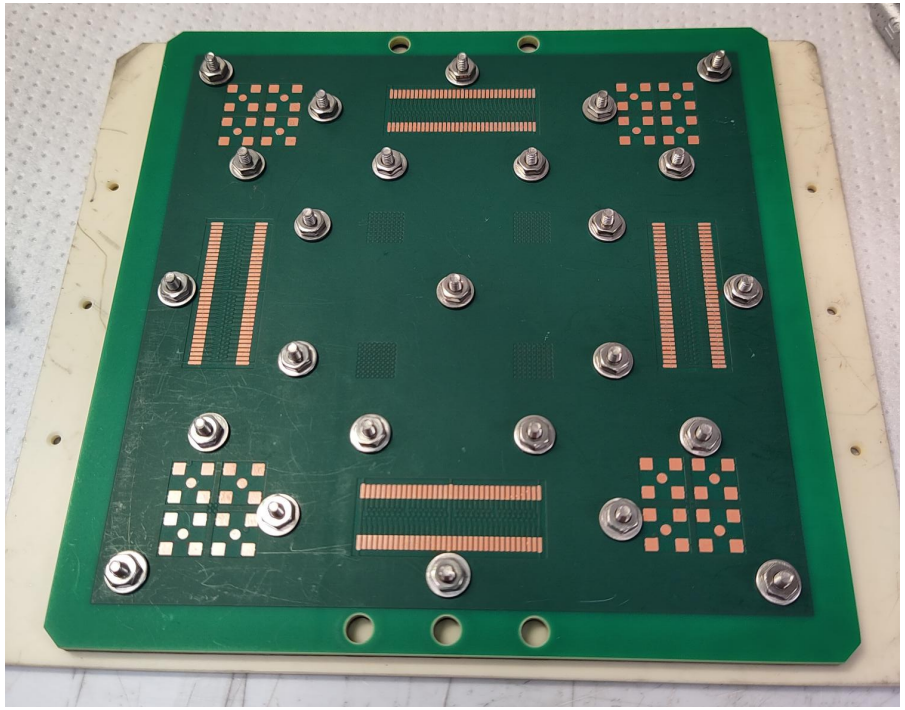
Case #1: double-sided (floating) 800 μm pitch Samtec interposers



Bottom (interposer) side



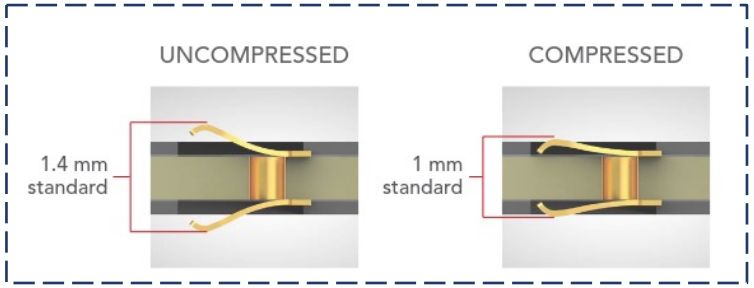
3D printed spacer, screws, interposers



Full assembly; top (connector) side

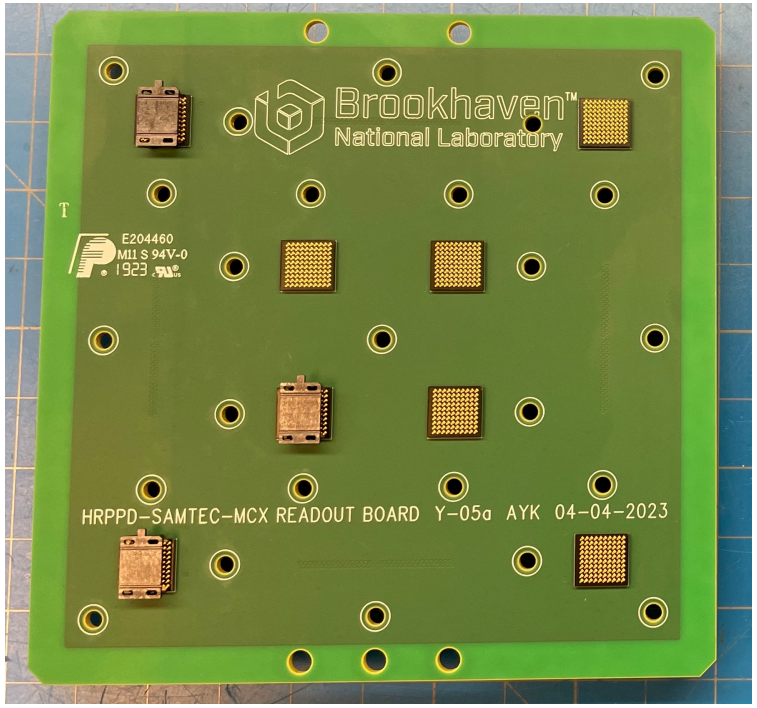
-> Electrical connectivity is confirmed,
as well as mechanical integration overall

Next step: signal quality check

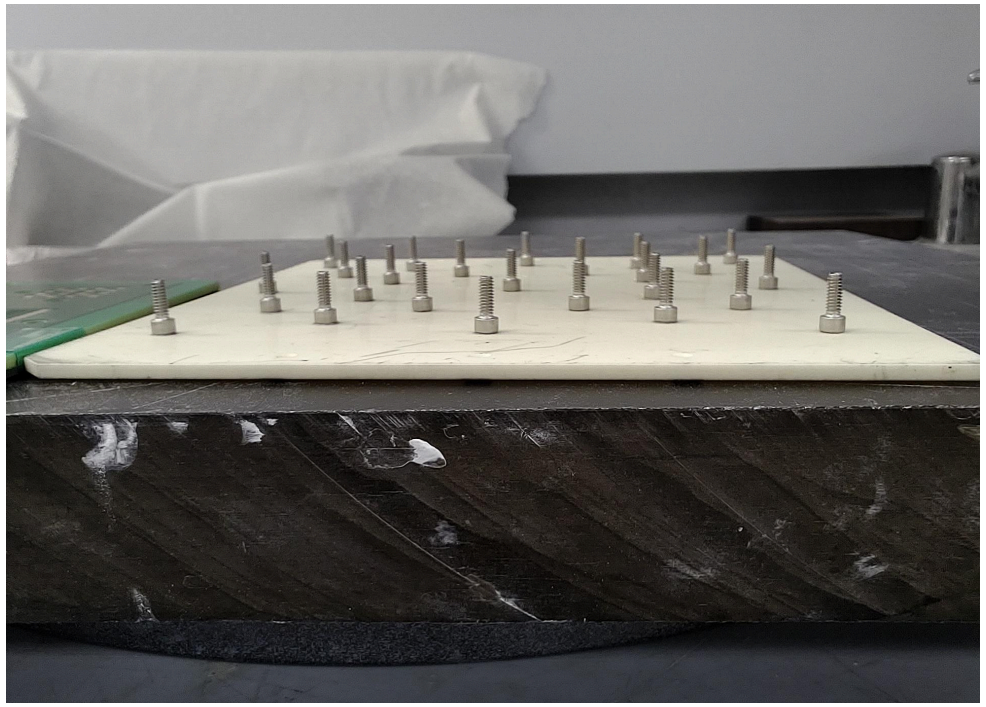


First iteration: a matching Y05a connector board

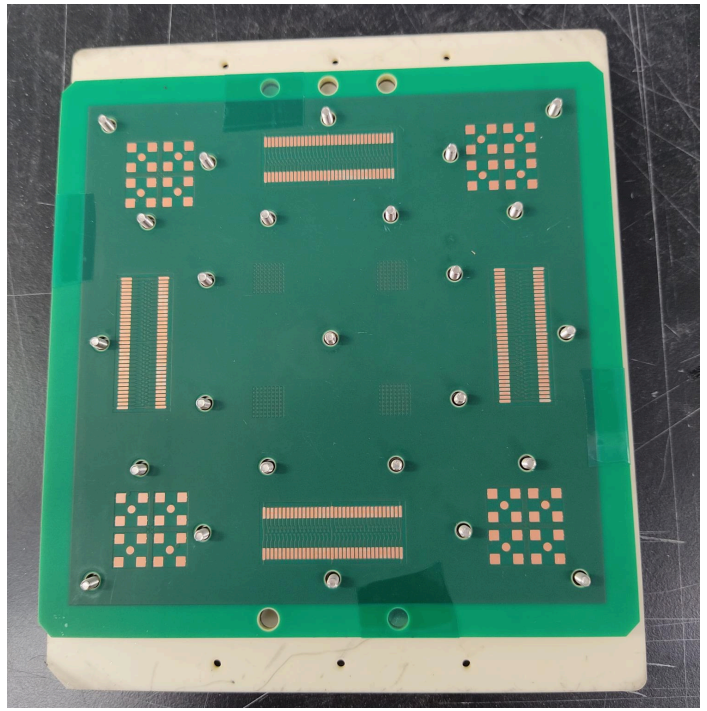
Case #2: single-sided (soldered) 800 μm pitch Samtec interposers



Bottom (interposer) side

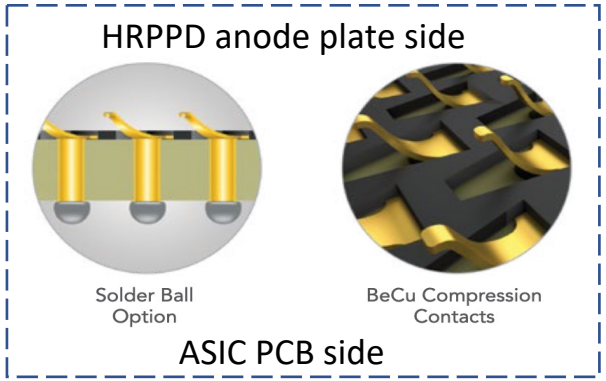


Screws epoxy glued onto a dummy ceramic plate



Top (connector) side

-> Have not been tried out yet
(but is not a leading option either)



ASIC considerations

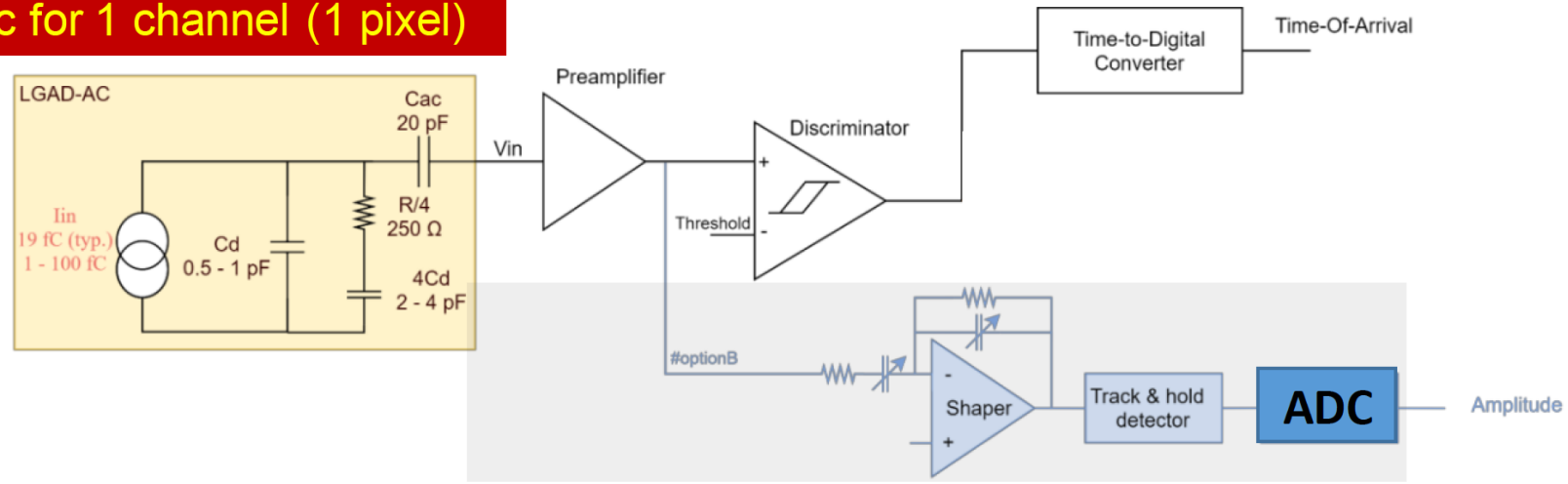
EICROC0 design: 16 channels (4x4)

Requirements:
- pixel size **0.5 x 0.5 mm²** ***(HGTD 1.3x1.3 mm²)***
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**

Charge sharing studies (simulation + β source)

EICROC0 design:
- TZ Preamplifiers from ALTIROC
- TDC from HGCROC (CMS, CEA/Irfu/DEDIP)
- 8 bit ADC for time-walk correction (AGH Krakow, adapted from HGCROC)

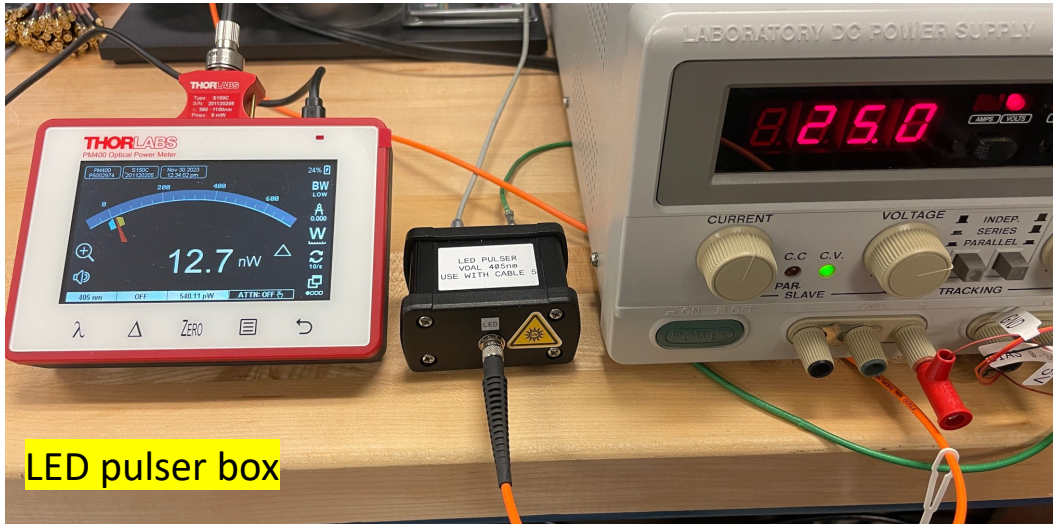
Schematic for 1 channel (1 pixel)



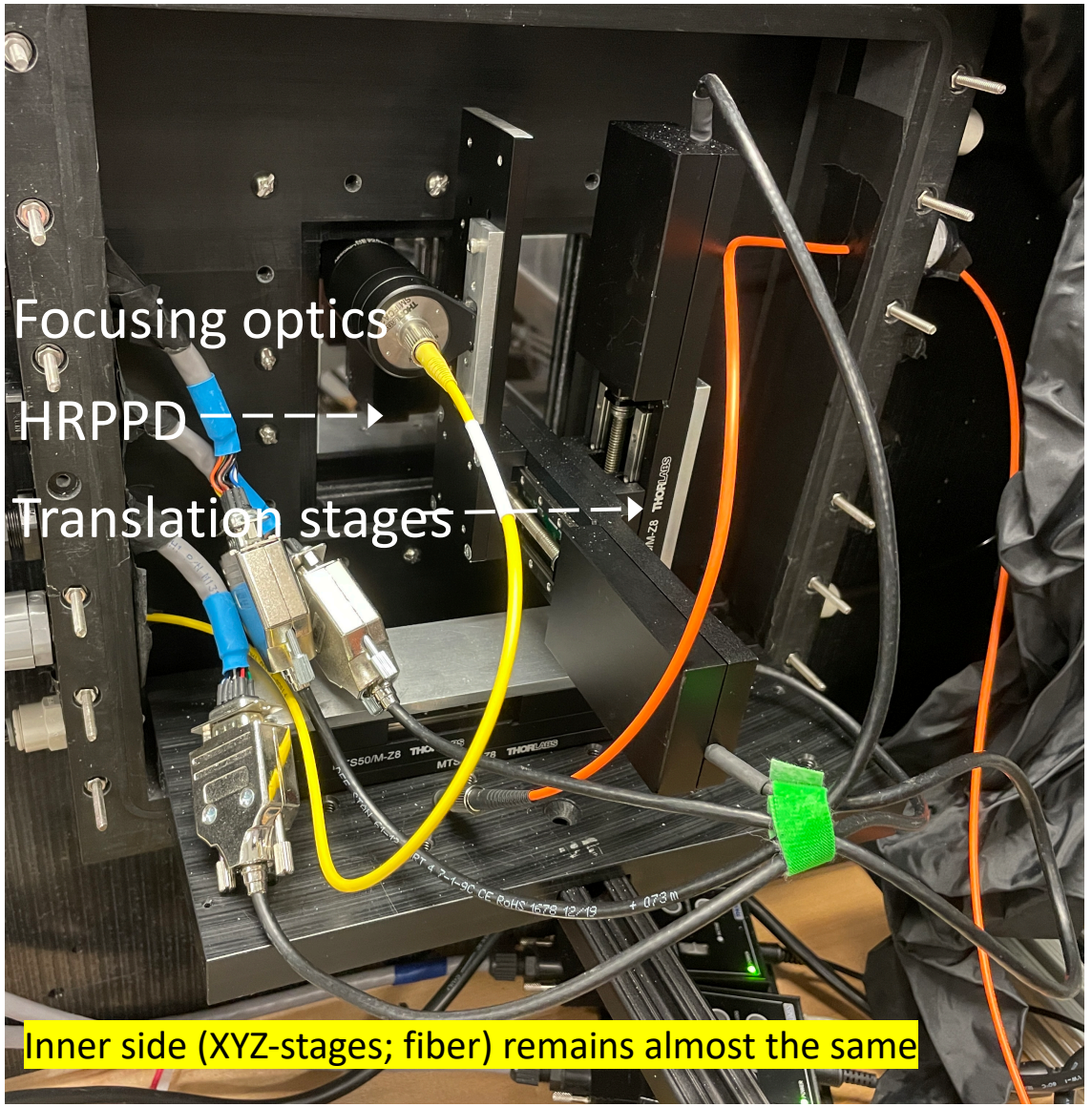
Compared to ALTIROC, ToT TDC (non-linear behavior as a function of deposited charge) replaced by an ADC

HRPPD QA station @ BNL

- Consolidate all HRPPD-related equipment in a new lab space
  - A slightly modified existing dark box
    - 2” XY-translation stages (>52mm travel) suffice to scan a single quadrant of a 104mm x 104mm HRPPD active area at a time, pixel by pixel
  - PiLas (picosecond) and Elmo (femtosecond) lasers
  - DAQ PC, NIM & VME crates, 8x V1742s
  - LED pulser box by Fernando [for QE measurements]



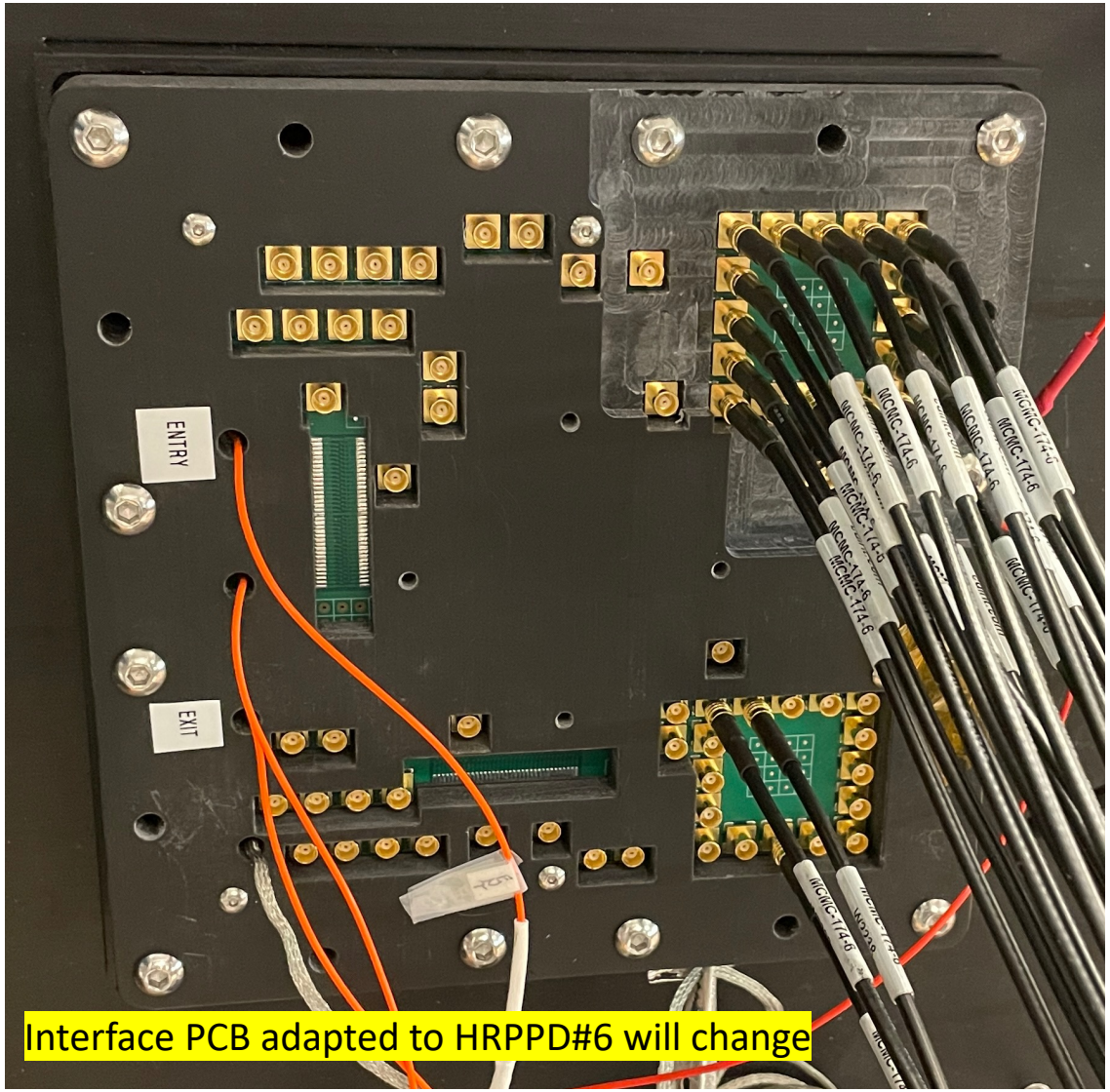
LED pulser box



Inner side (XYZ-stages; fiber) remains almost the same

HRPPD QA station @ BNL

- Optimize data taking procedure
  - Synchronize DRS4 configuration with the XY-stage positioning (we are interested only in the illuminated pad data for these scans)
  - Read out only one of the 8x4 DRS4 chips and only the first 136 out of 1024 samples at 5GS/s (event size reduction from ~50kB to <2kB)
  - Then both the data volume and the CPU needs are manageable (assume 10^5 events per pixel @ ~5kHz, with ~5% single photon events)
- Plan to perform per pixel surface scans:
  - PDE (*in a counting mode*) & gain uniformity, timing
  - DCR in a self-triggering mode at 2.5GS/s (?)
  - QE via a direct photocathode current measurement



Interface PCB adapted to HRPPD#6 will change